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Fig. 1A

Prior Art

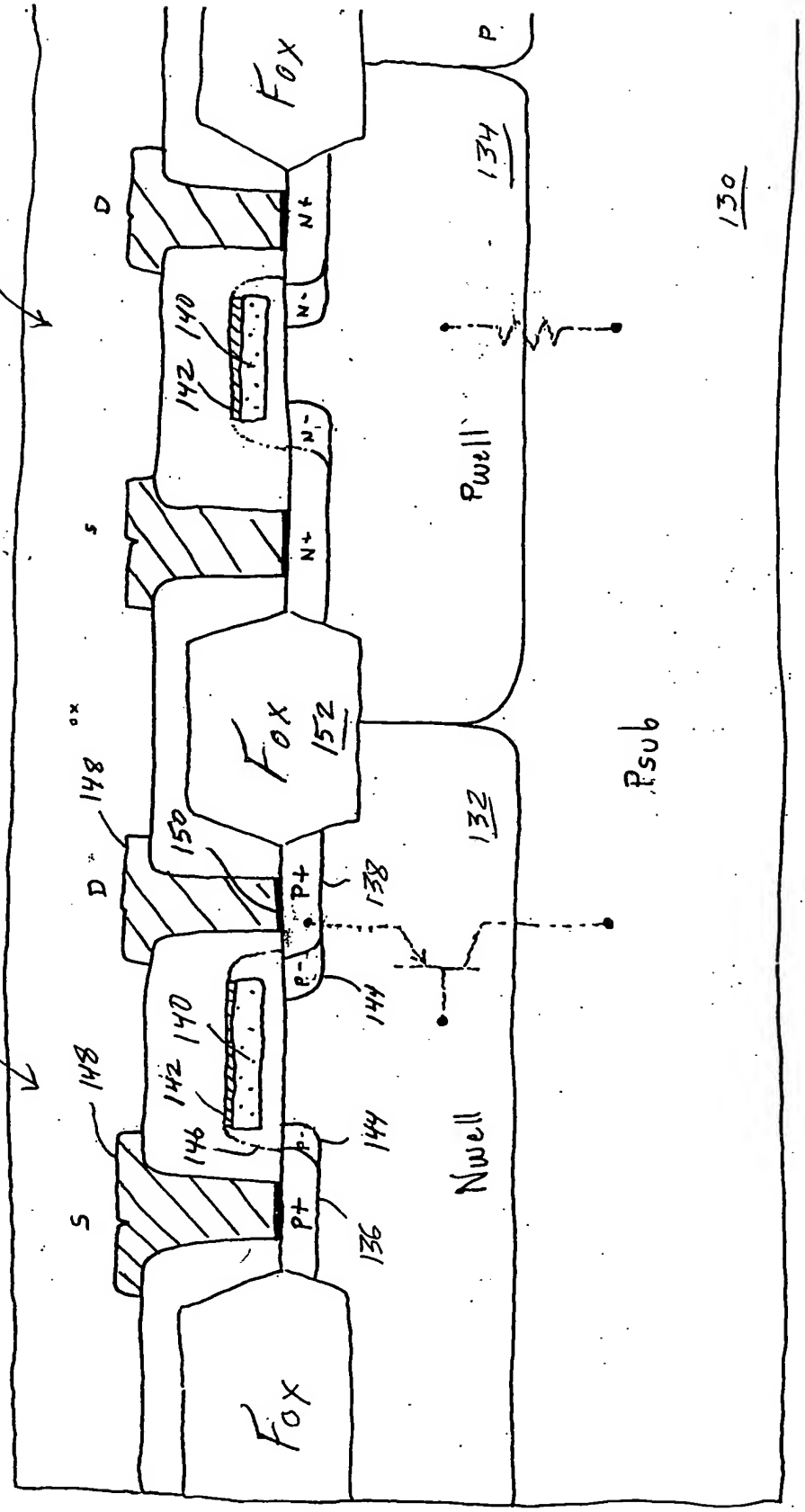


Fig. 1C
Prior Art

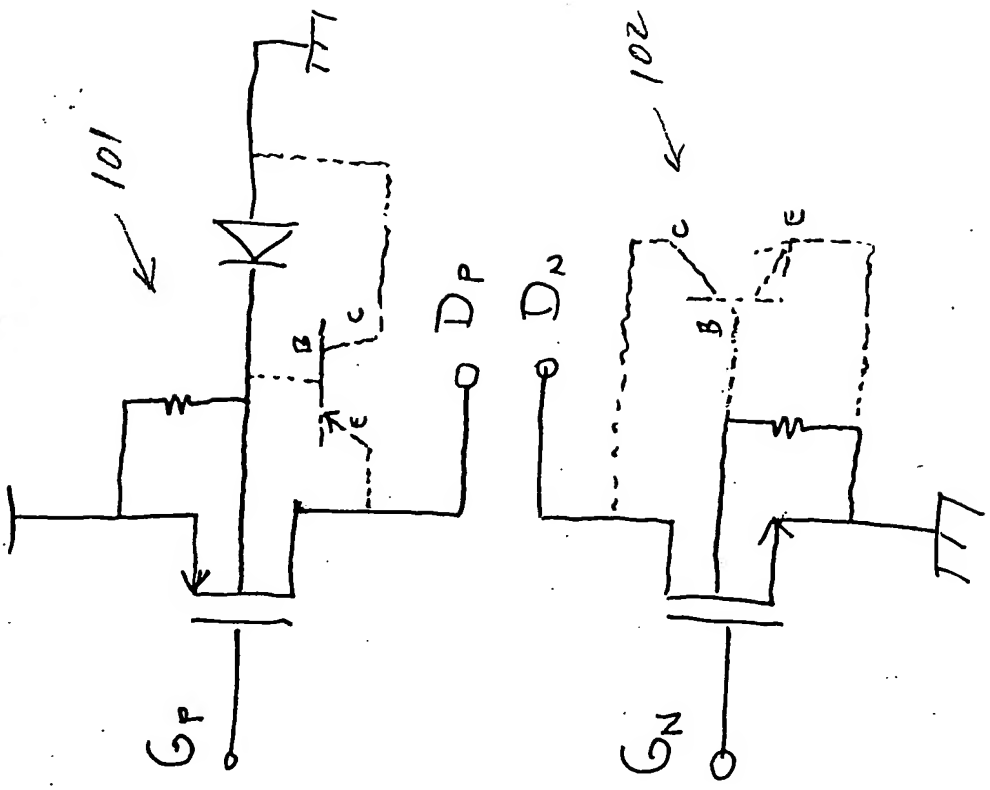
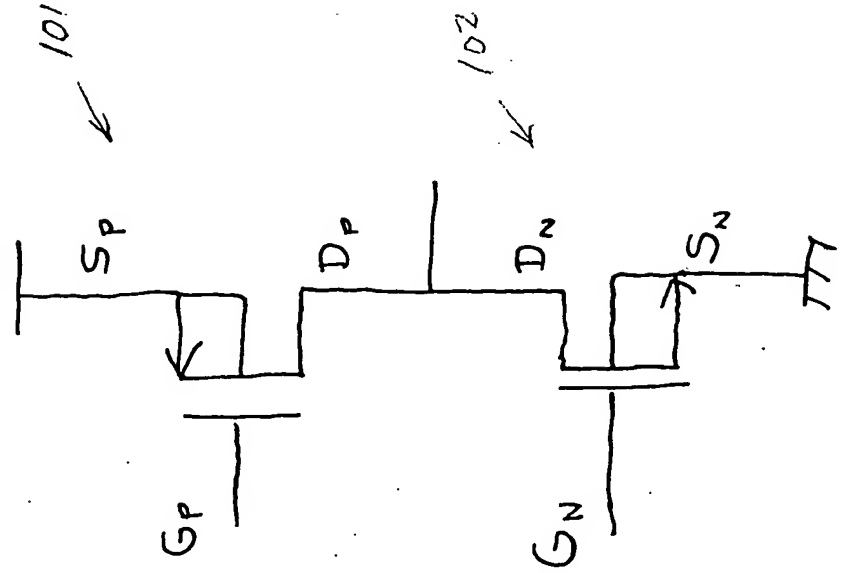


Fig. 1B
Prior Art



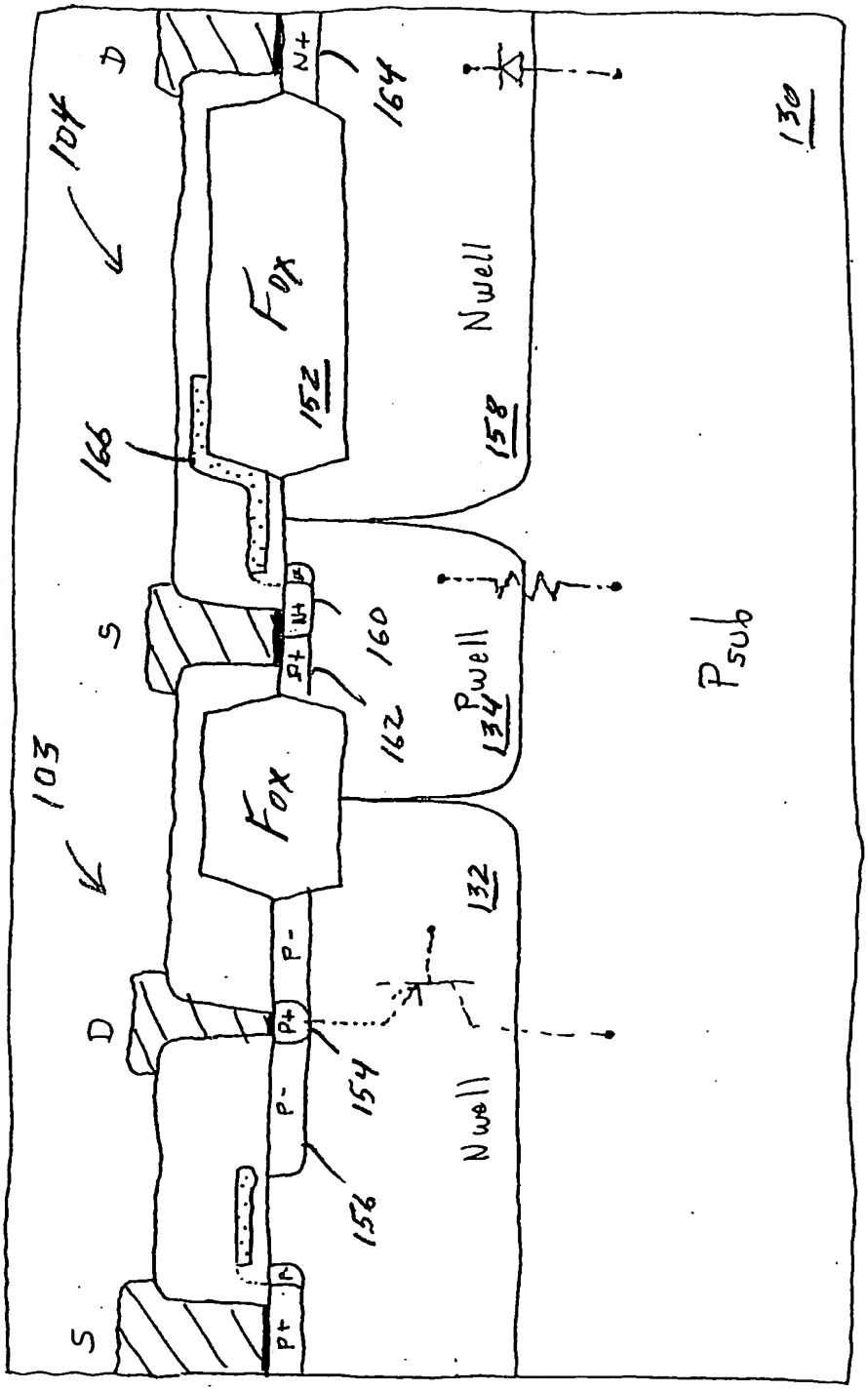

Prior Art
Fig. 2A
103
104
D
S
166
FOX
152
N+
164
Nwell
158
130
160
162
Pwell
134
Psub
132
P-
P+
154
156
Nwell

Fig. 2B

Prior Art

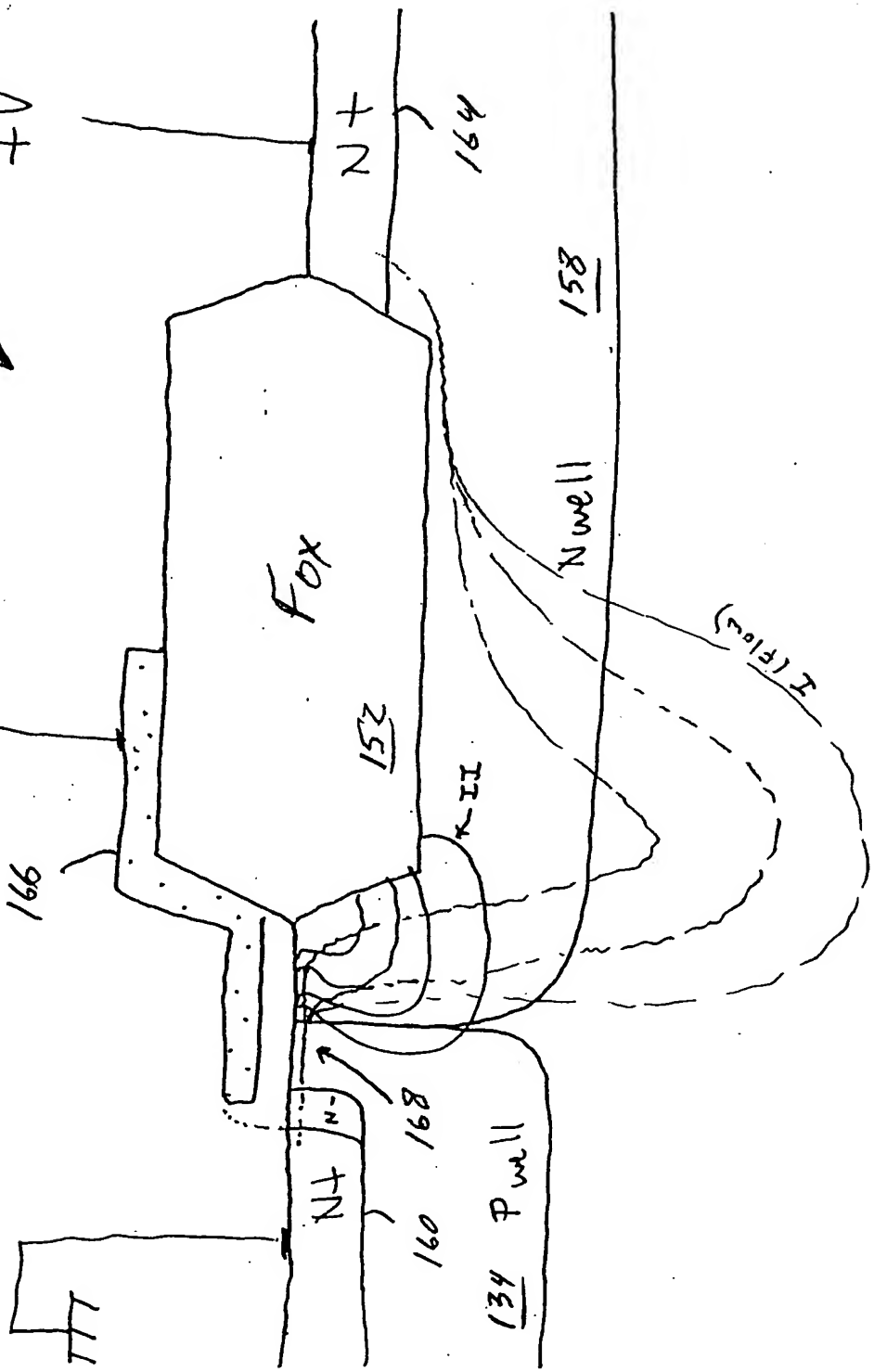
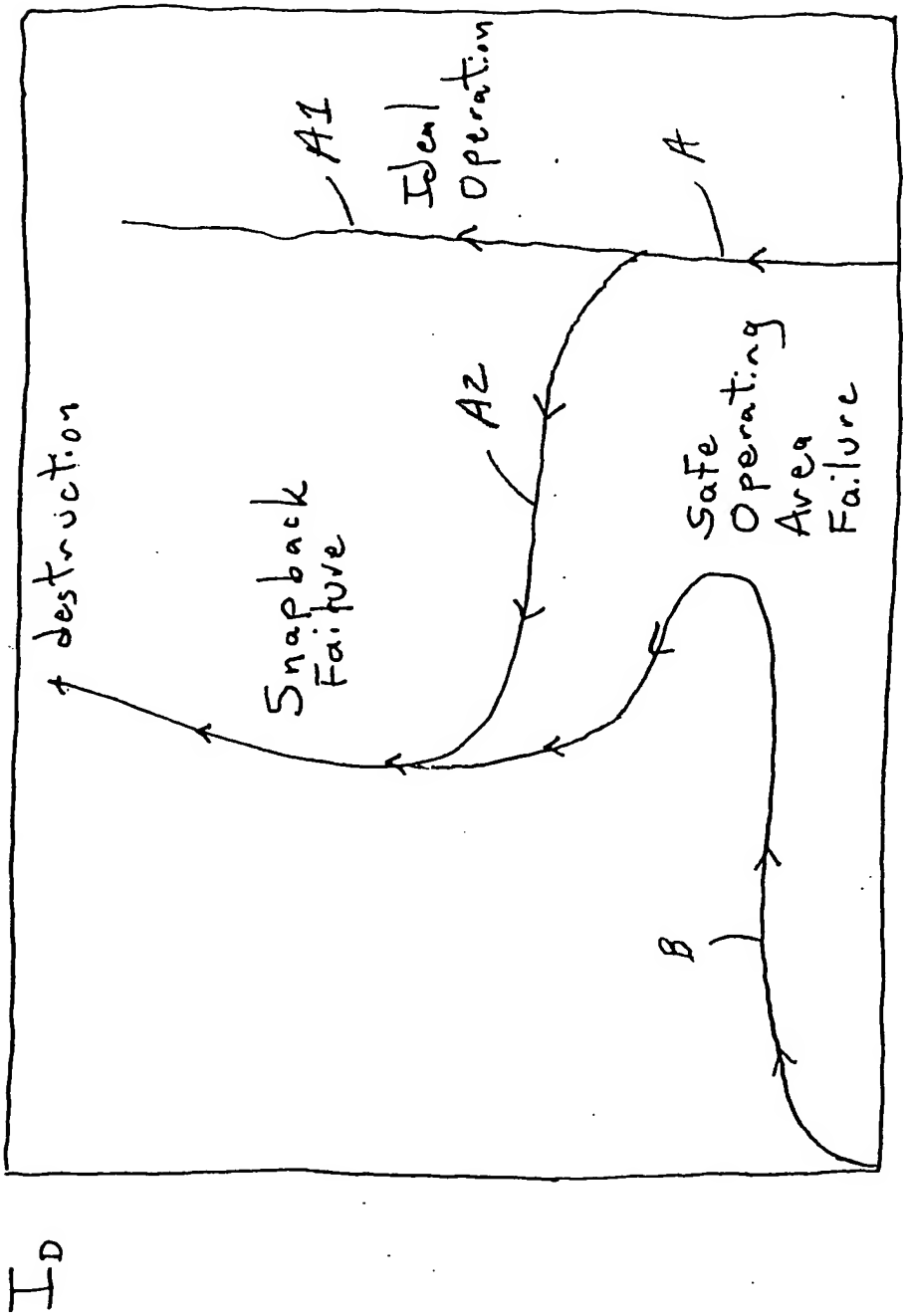


Fig 2C

Prior Art



Prior Art

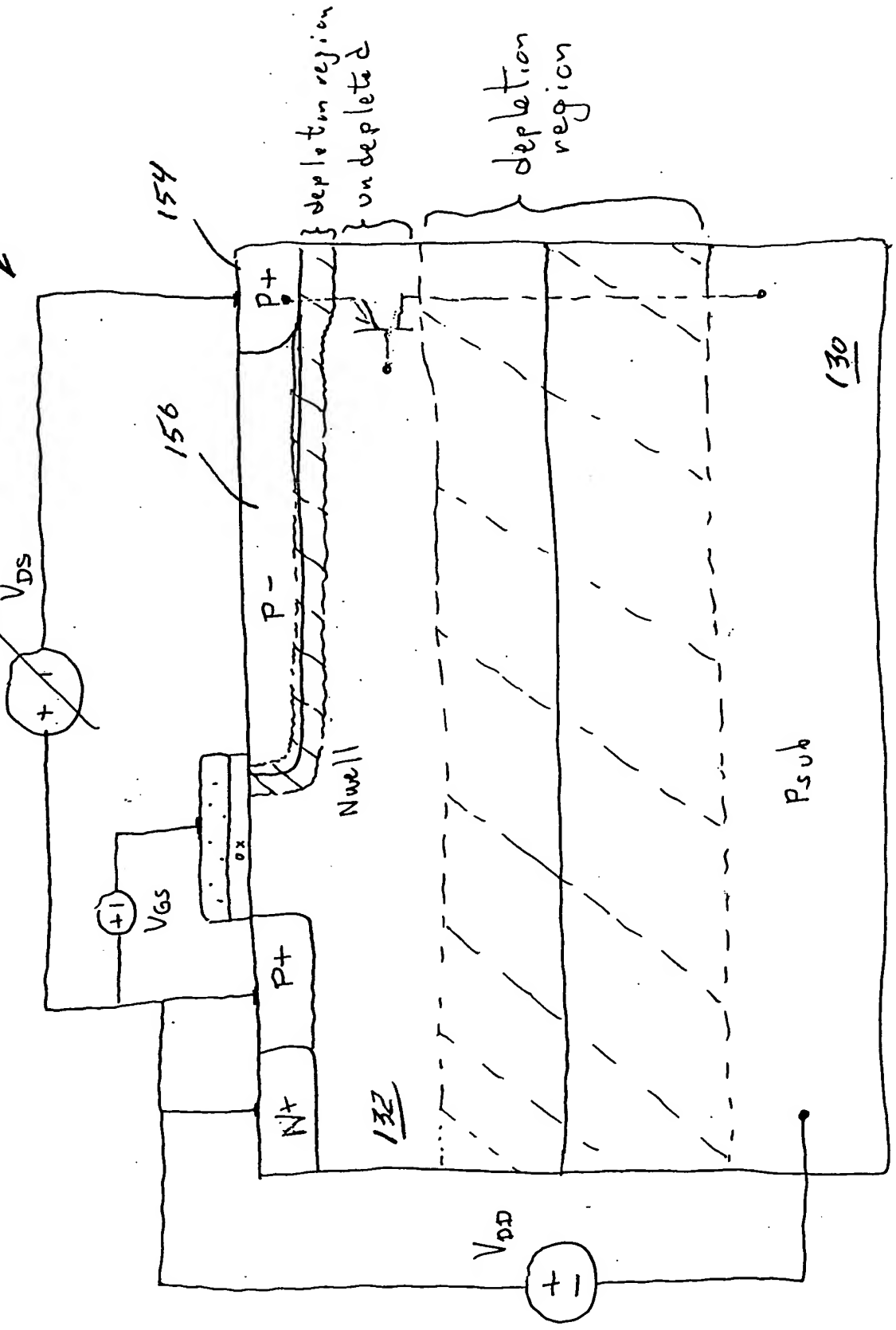
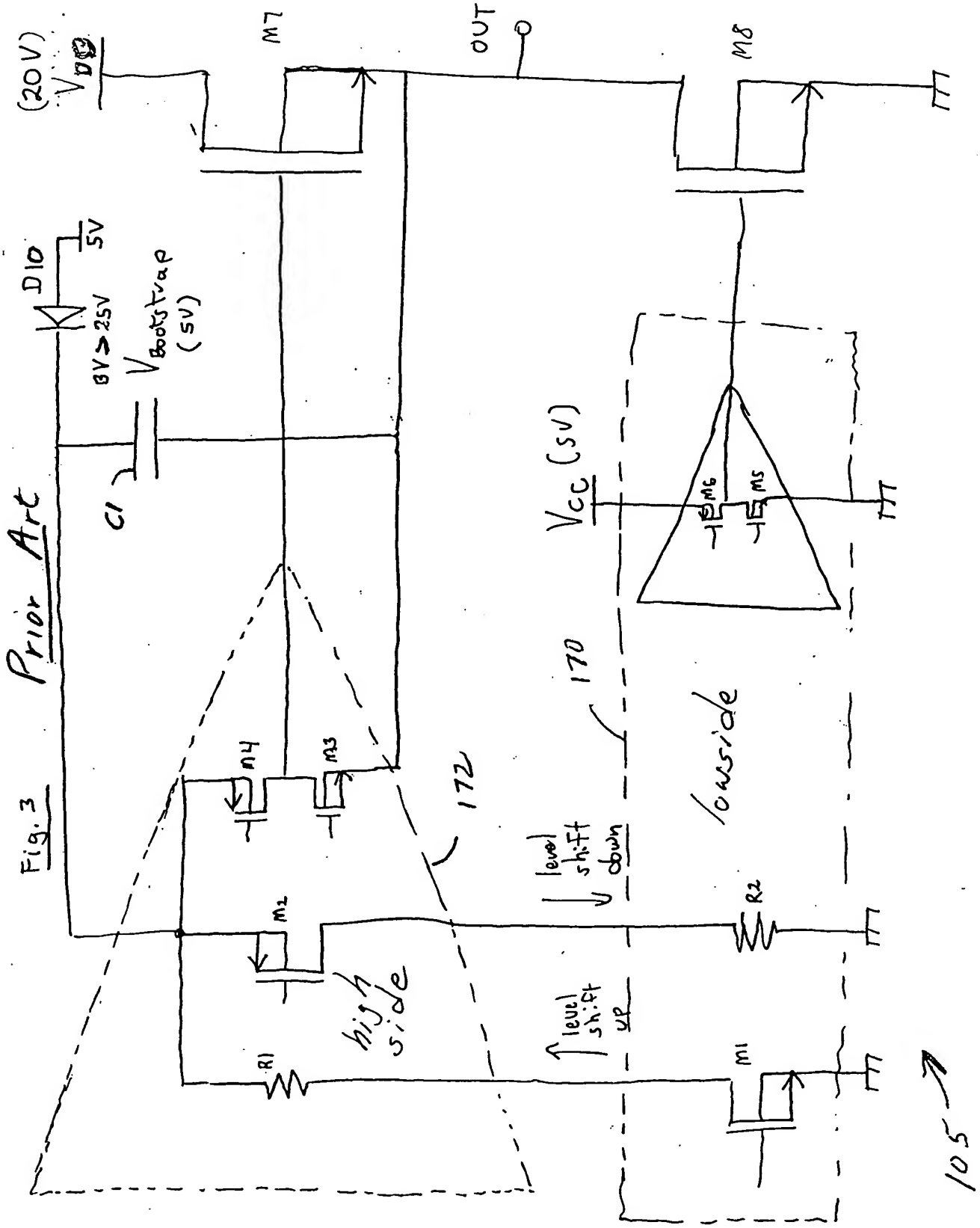


Fig. 2D



Prior Art

Fig. 3

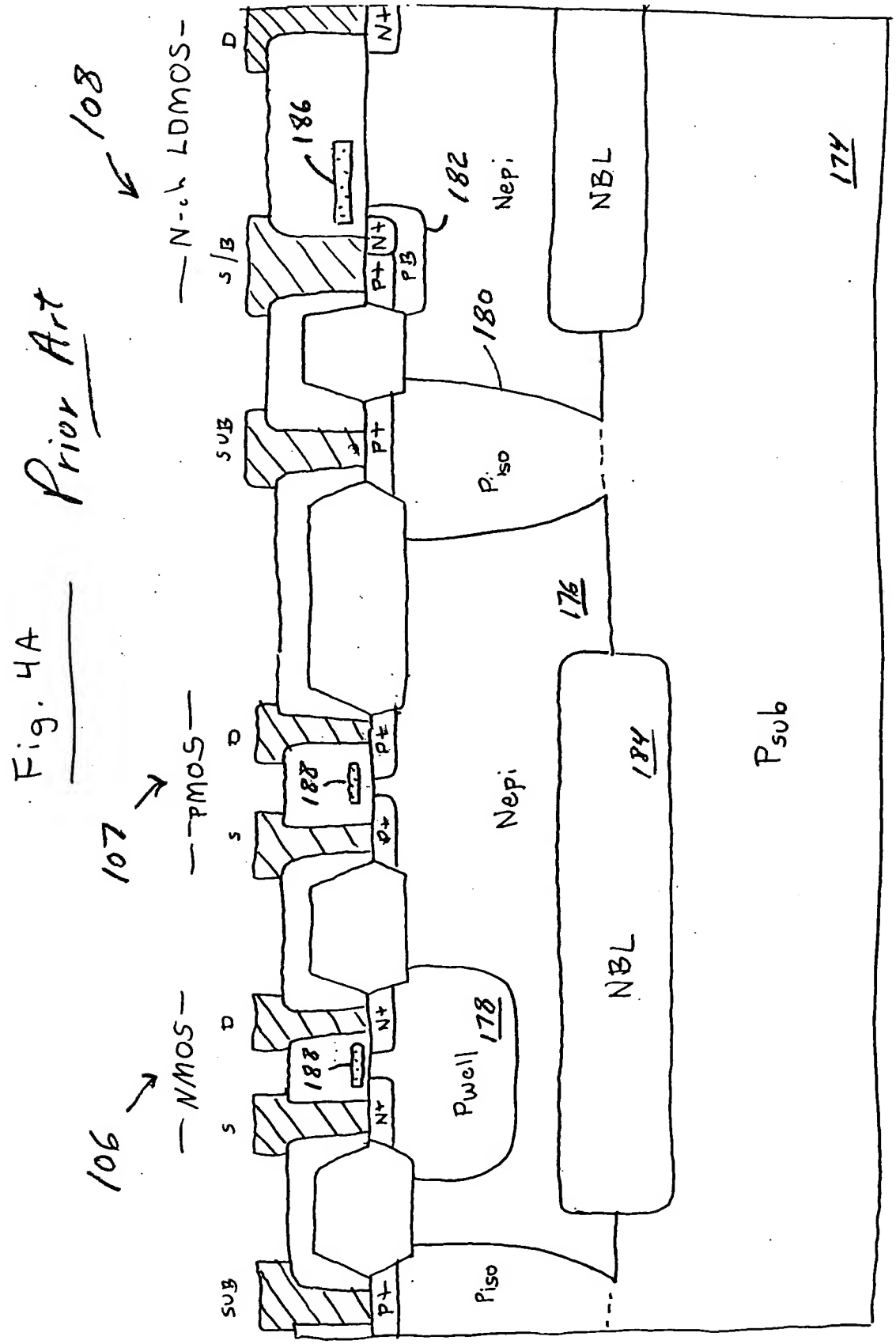
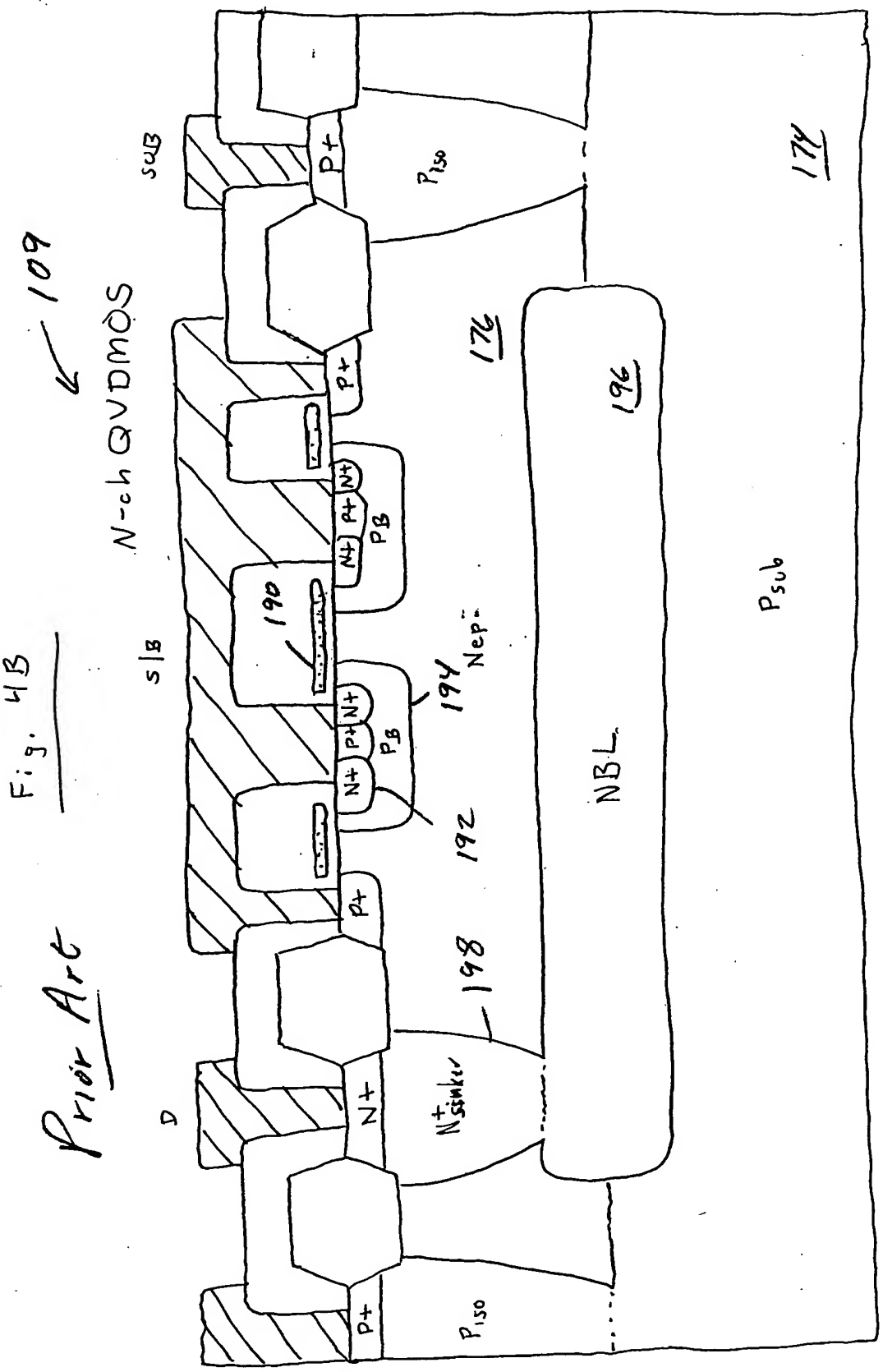
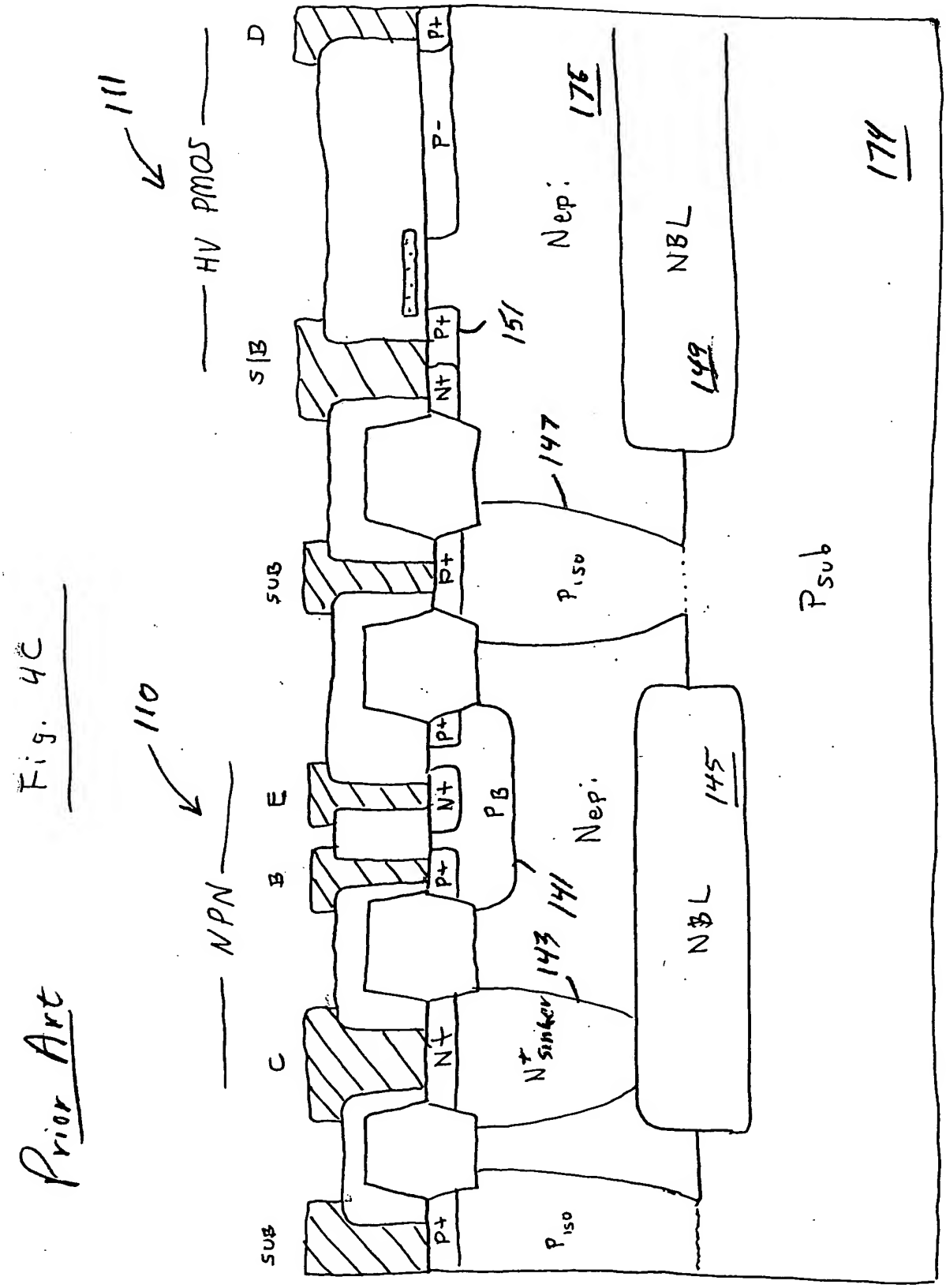


Fig. 4A Prior Art

Fig. 4B

Prior Art



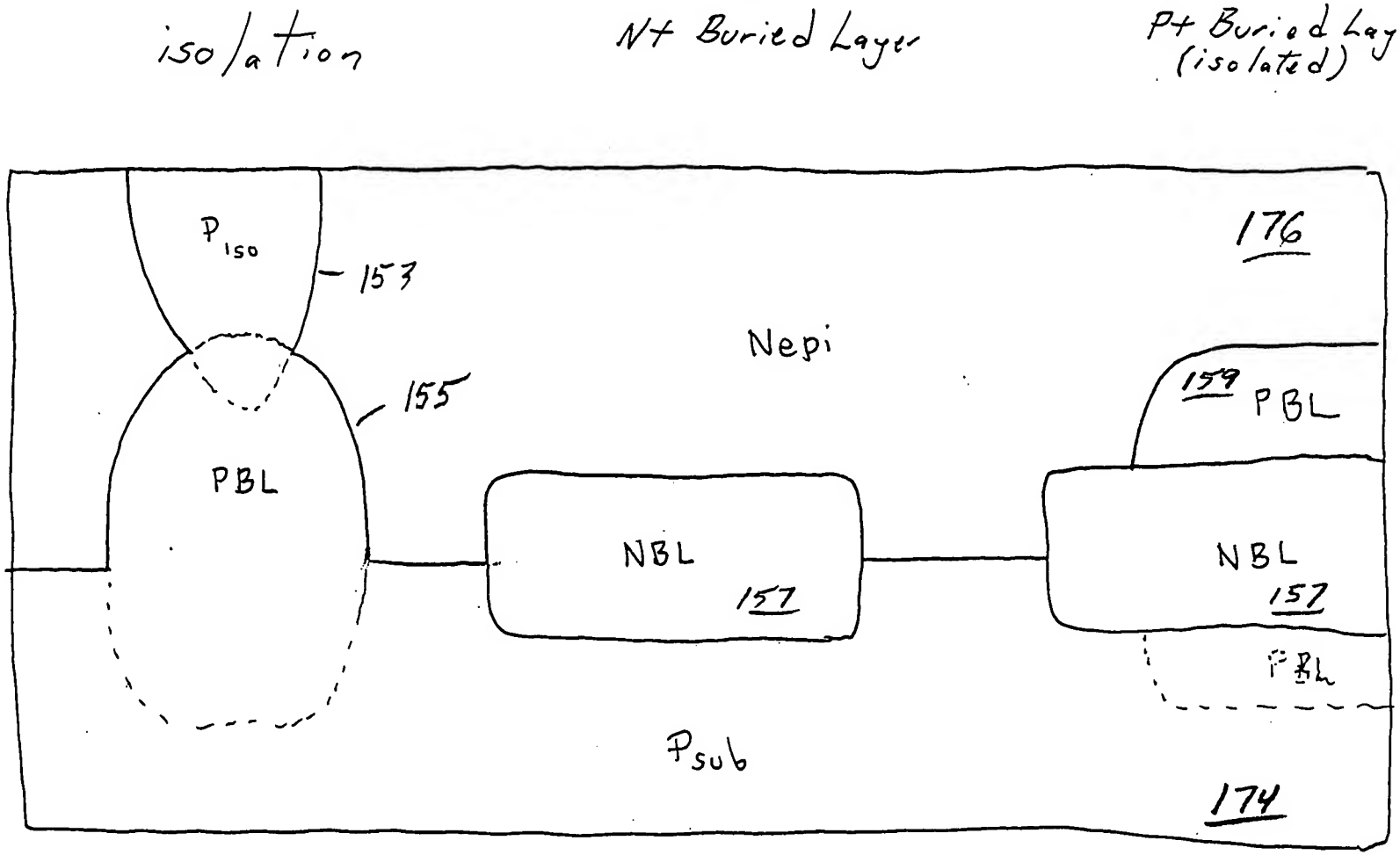


Prior Art

Fig. 4C

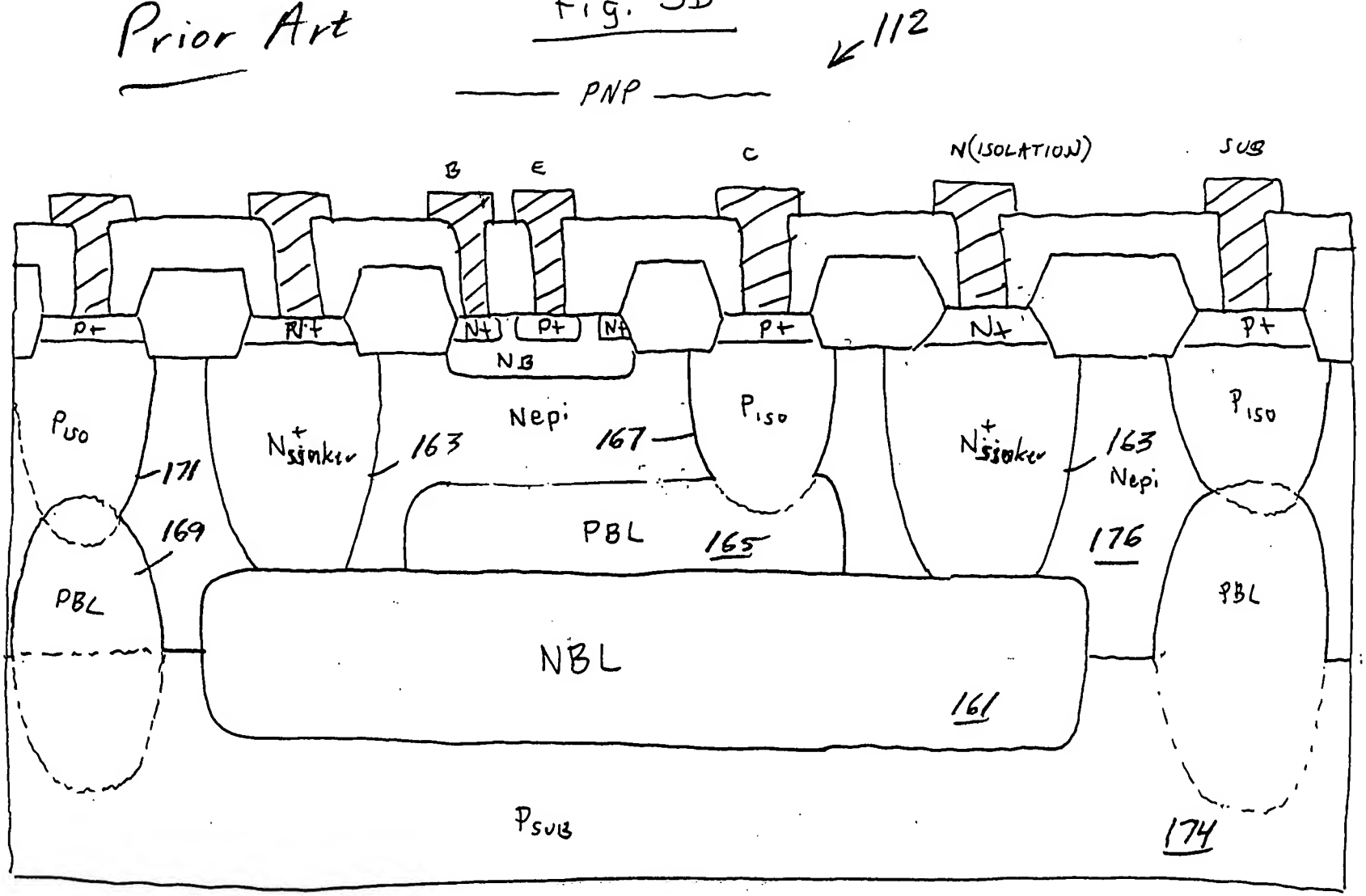
Prior Art

Fig: 5A



Prior Art

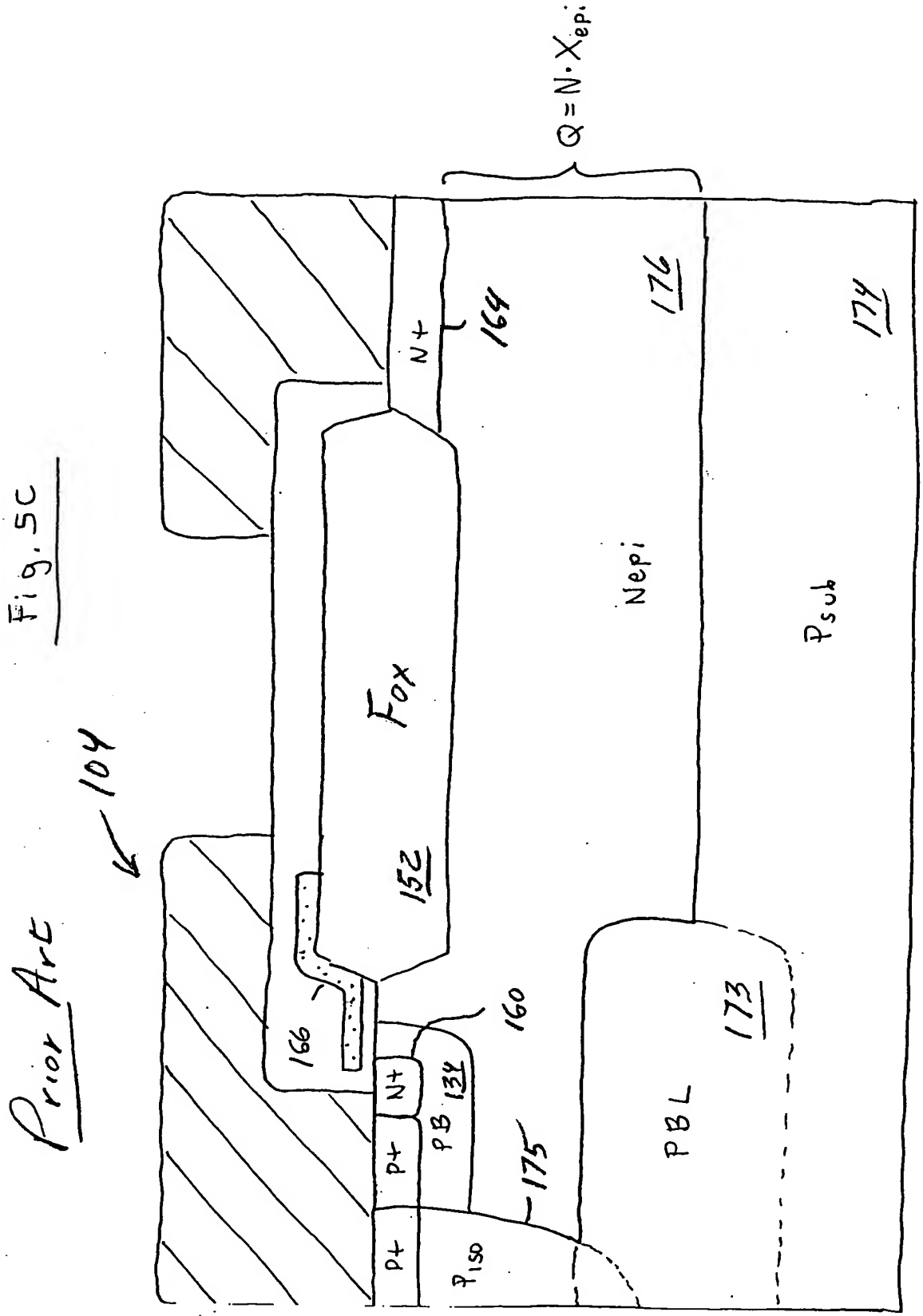
Fig. 5B



6/12/19

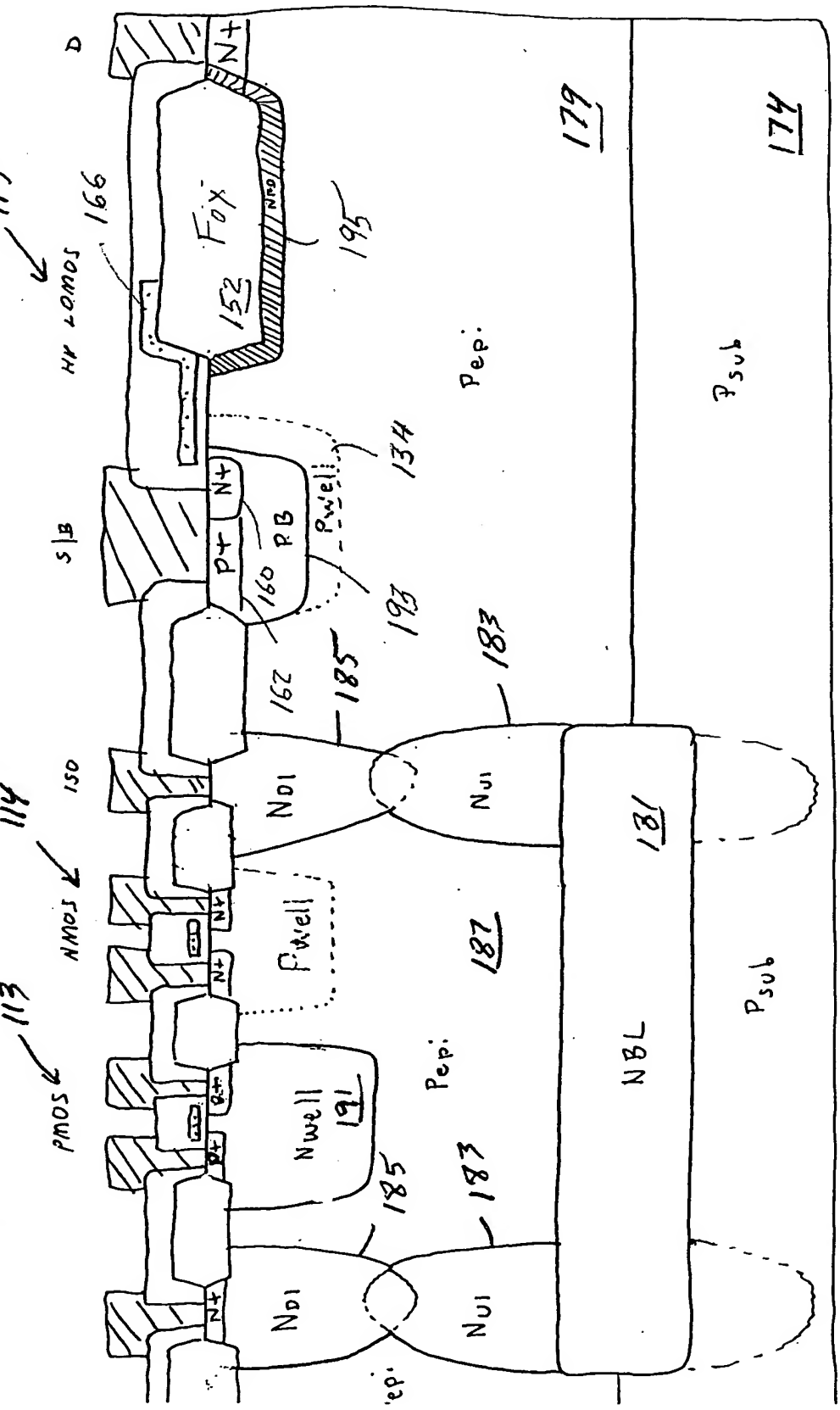
Fig. 5C

Prior Art



Prior Art

Fig 6A



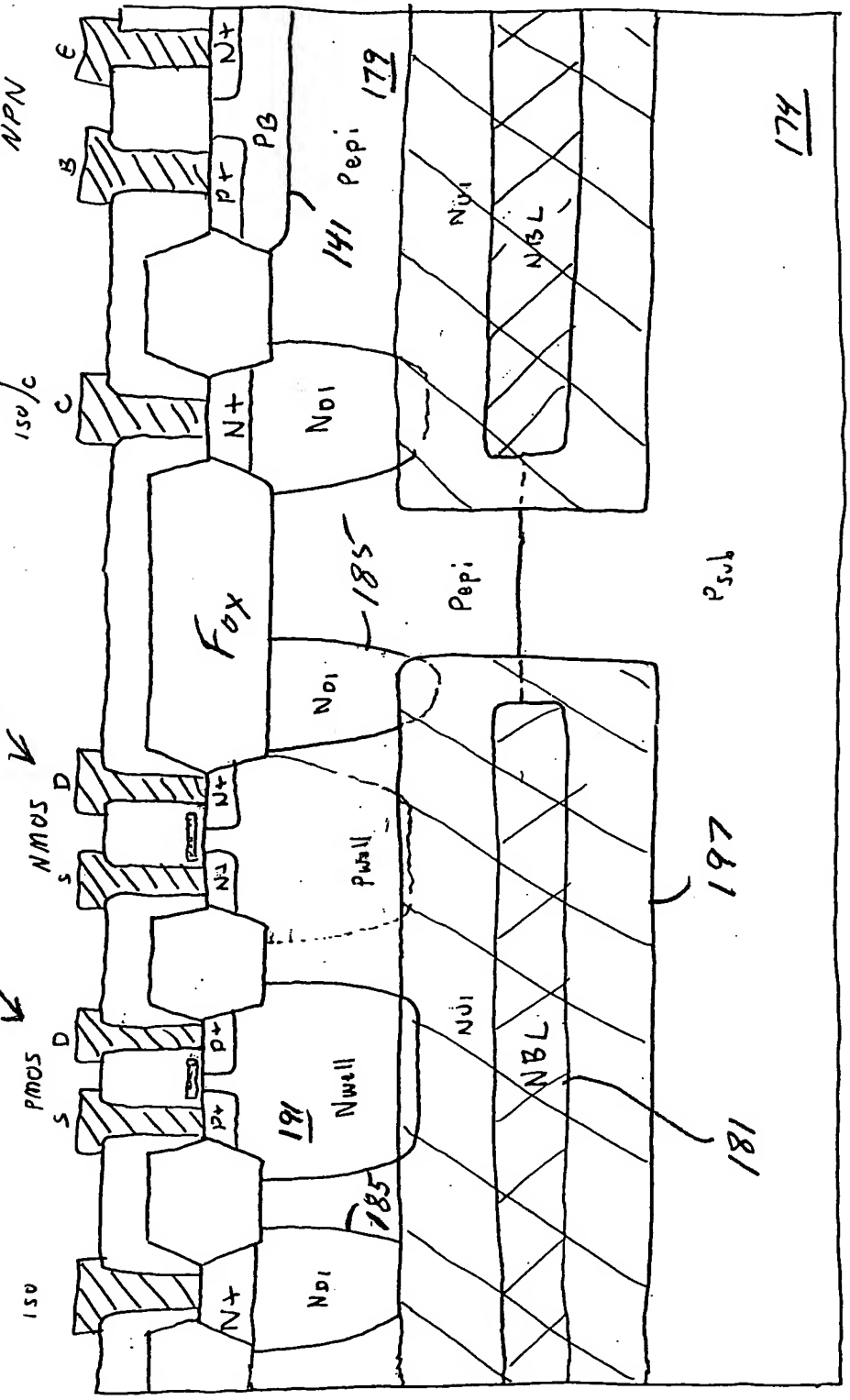


Fig. 6B

Prior Art

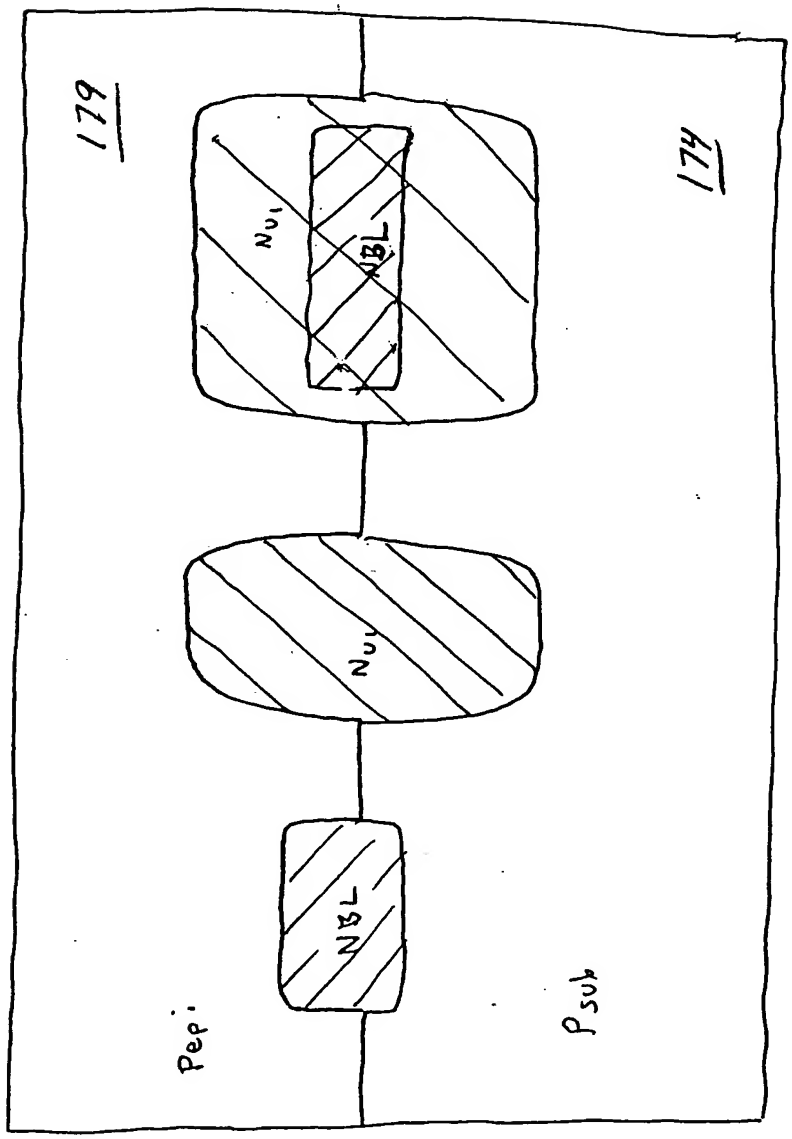


Fig. 6C

Prior Art

Prior Art

Fig. 7A

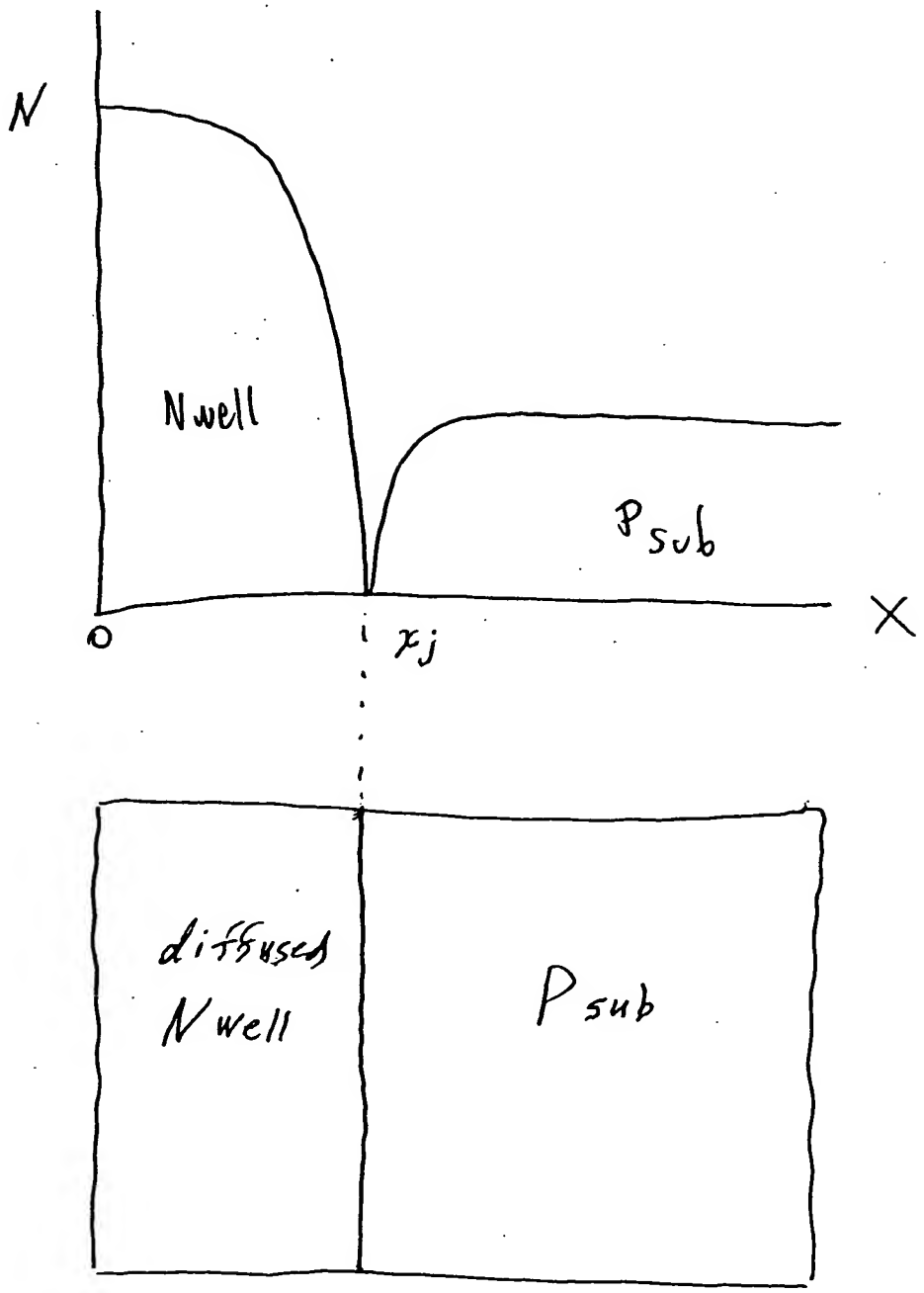


Fig. 7B

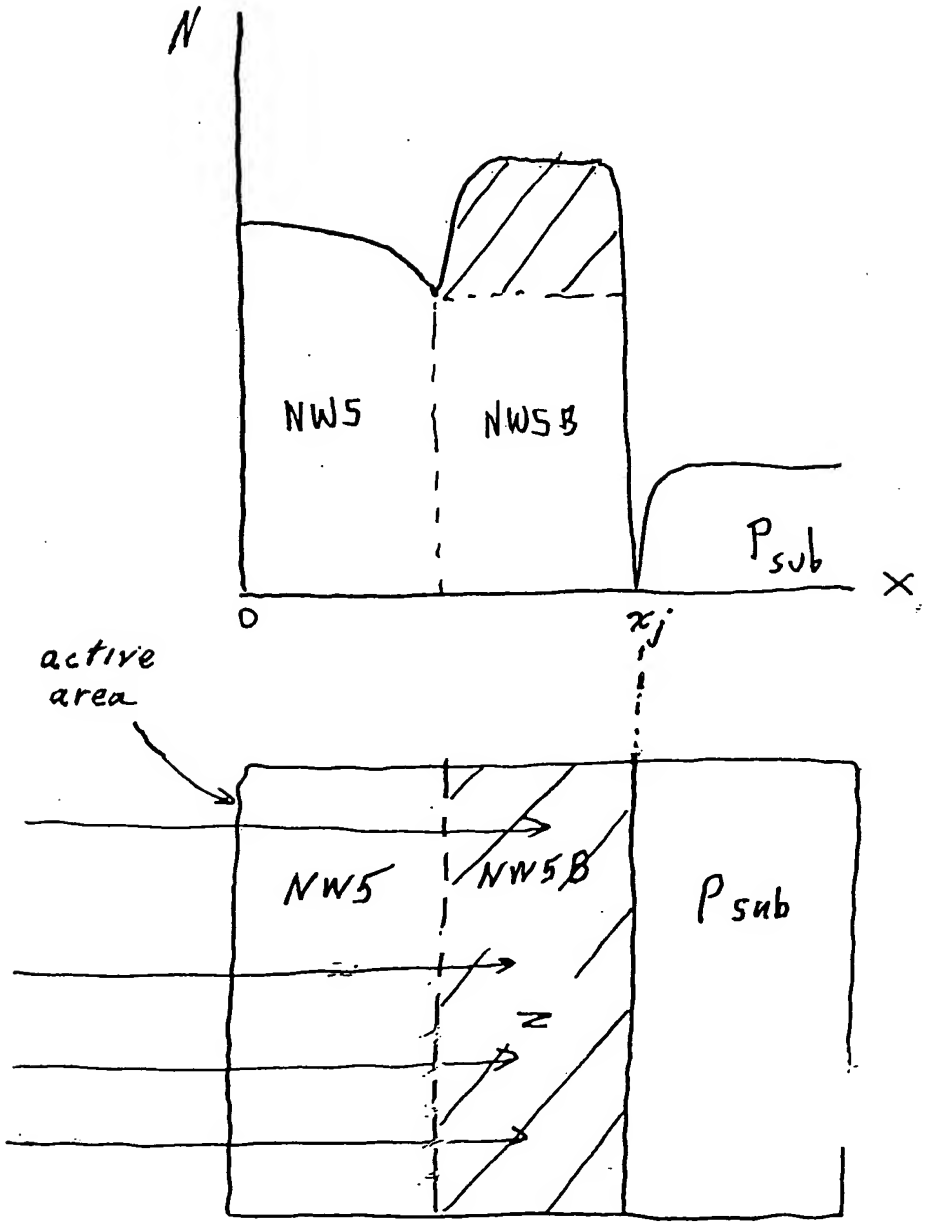


Fig. 7C

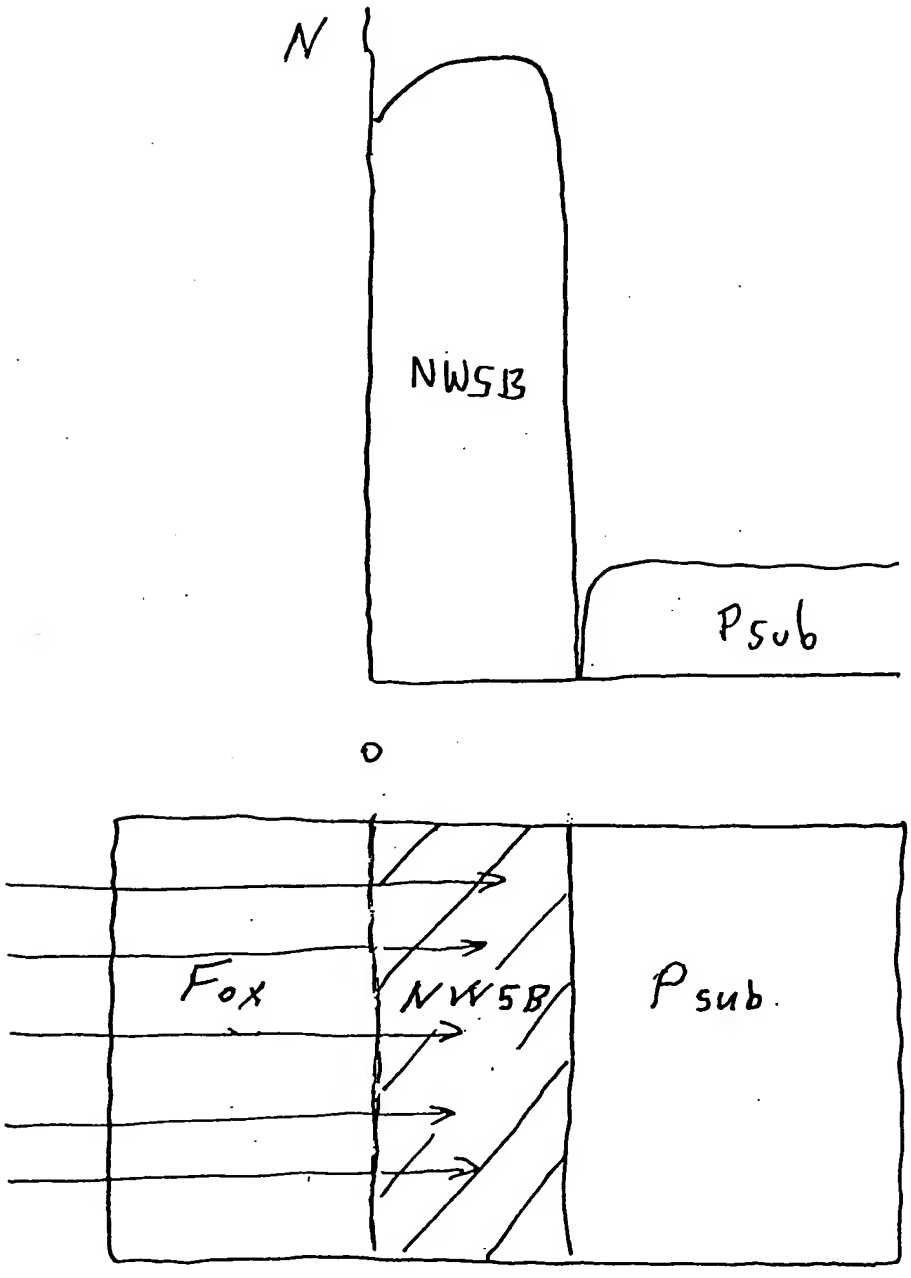


Fig. 8A

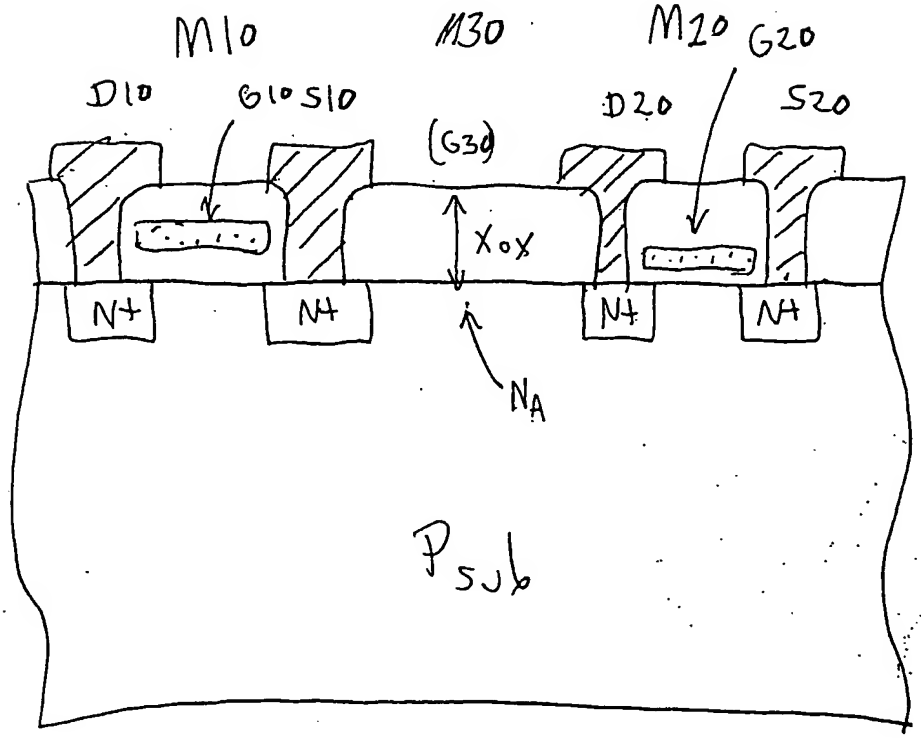

M10
M30
M20
G20
D10
G10
S10
D20
S20
(G30)
X_{OX}
N+
N+
N+
N+
N_A
P_{SUB}

Fig. 8B

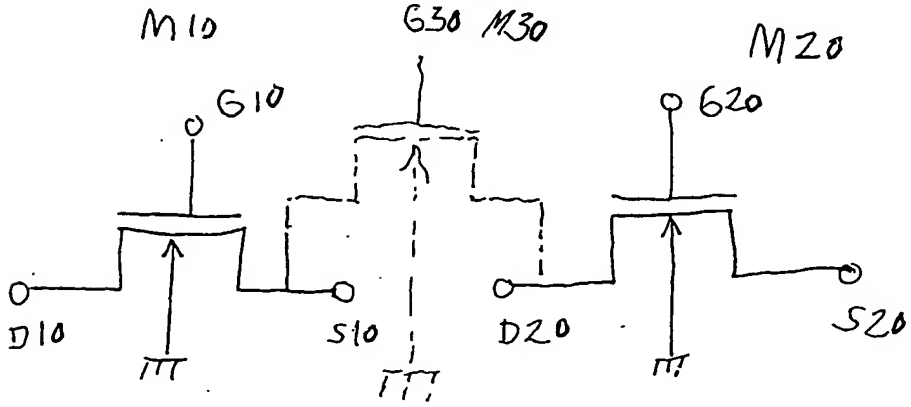
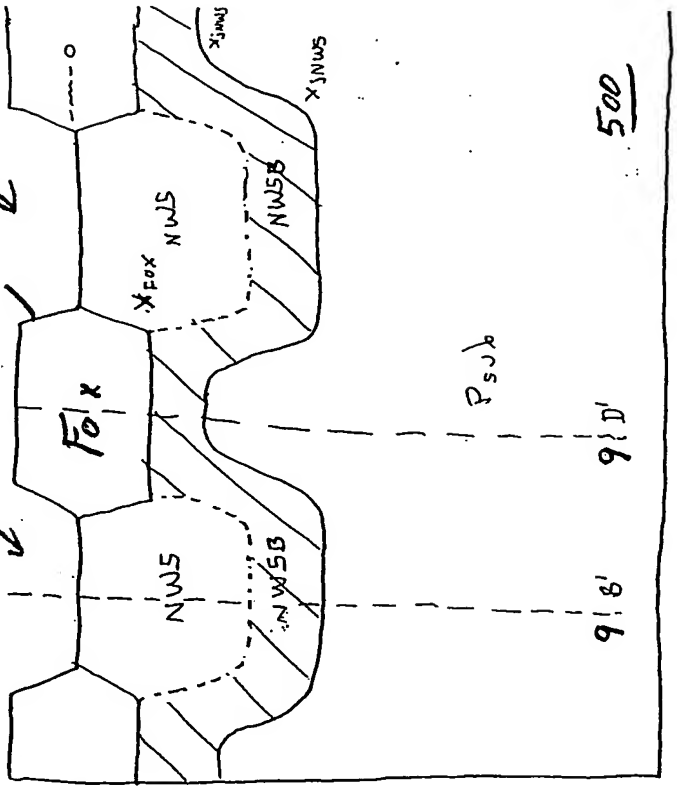
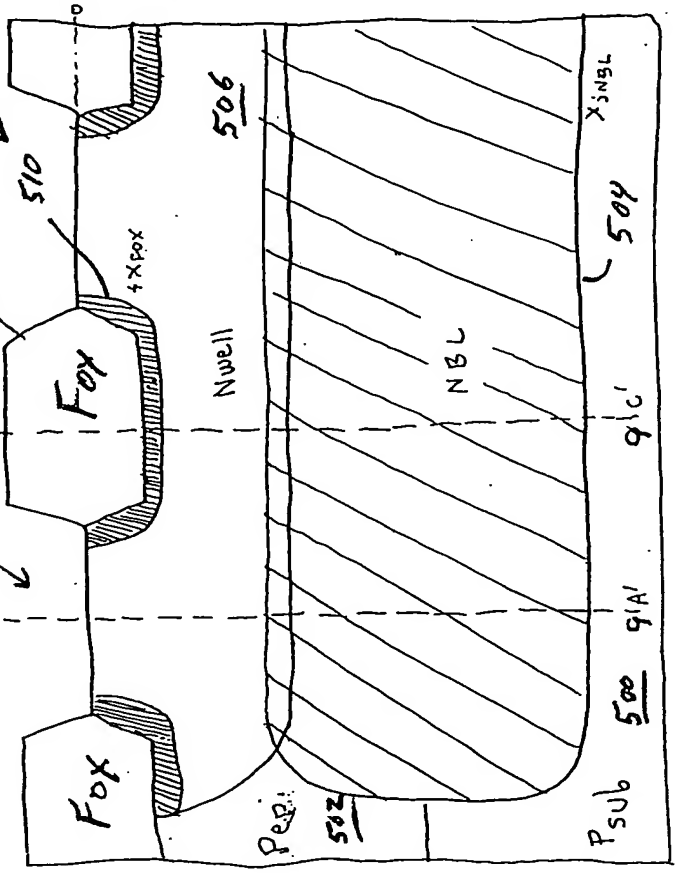

M10
G30
M30
M20
G10
G20
D10
S10
D20
S20

Fig. 9B



Prior Art

Fig. 9A



Prior Art

Fig. 9C

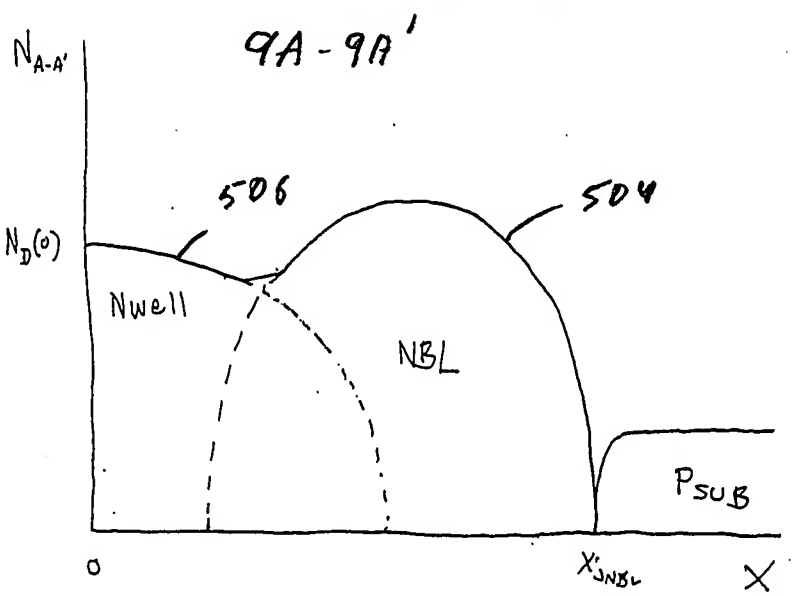
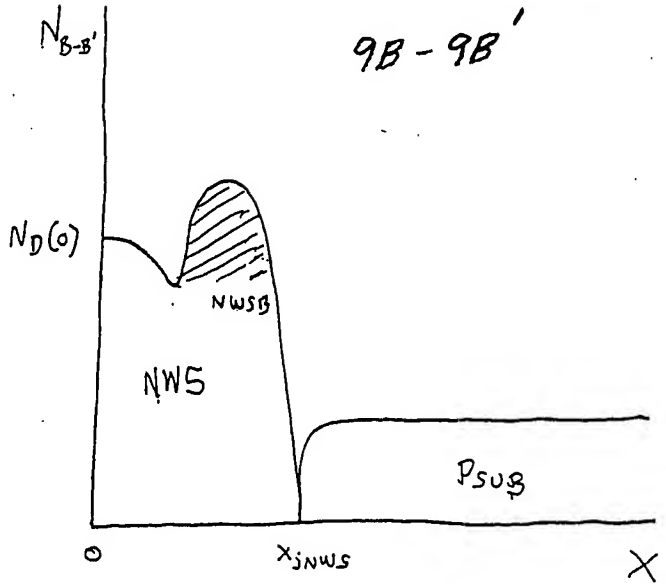


Fig. 9D



Prior Art

Fig. 9E

9C-9C'

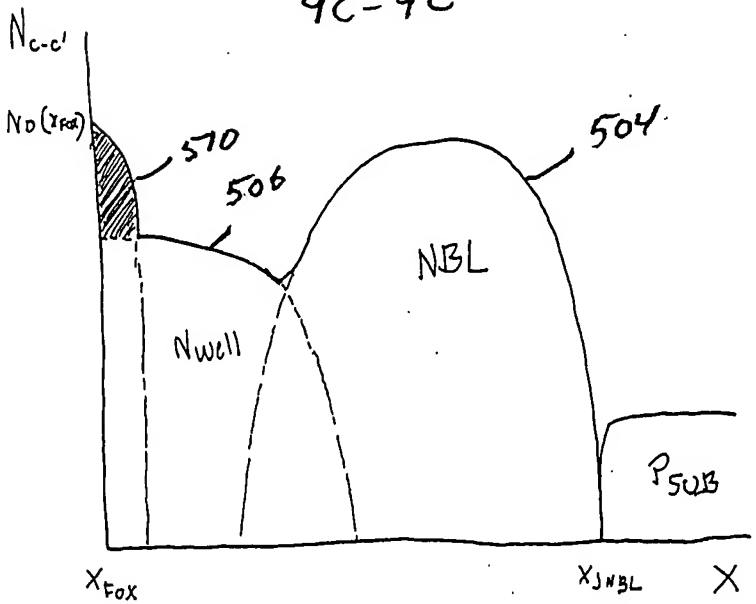
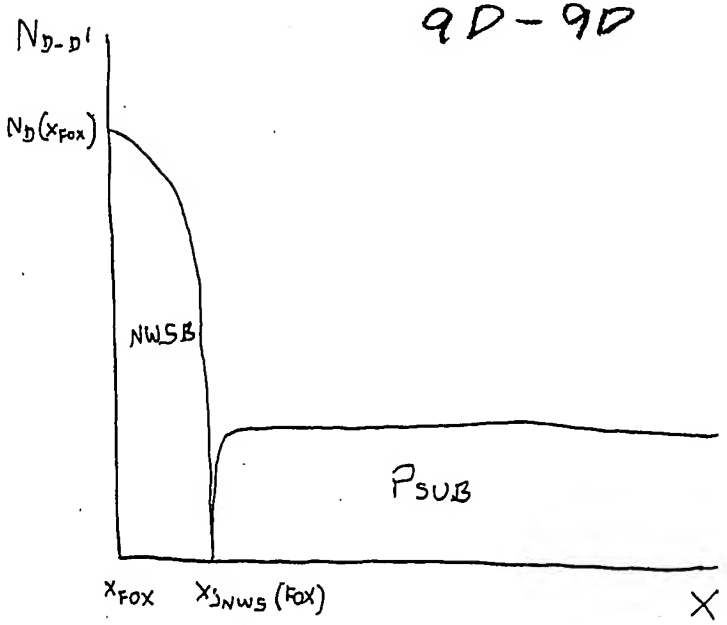


Fig. 9F

9D-9D'



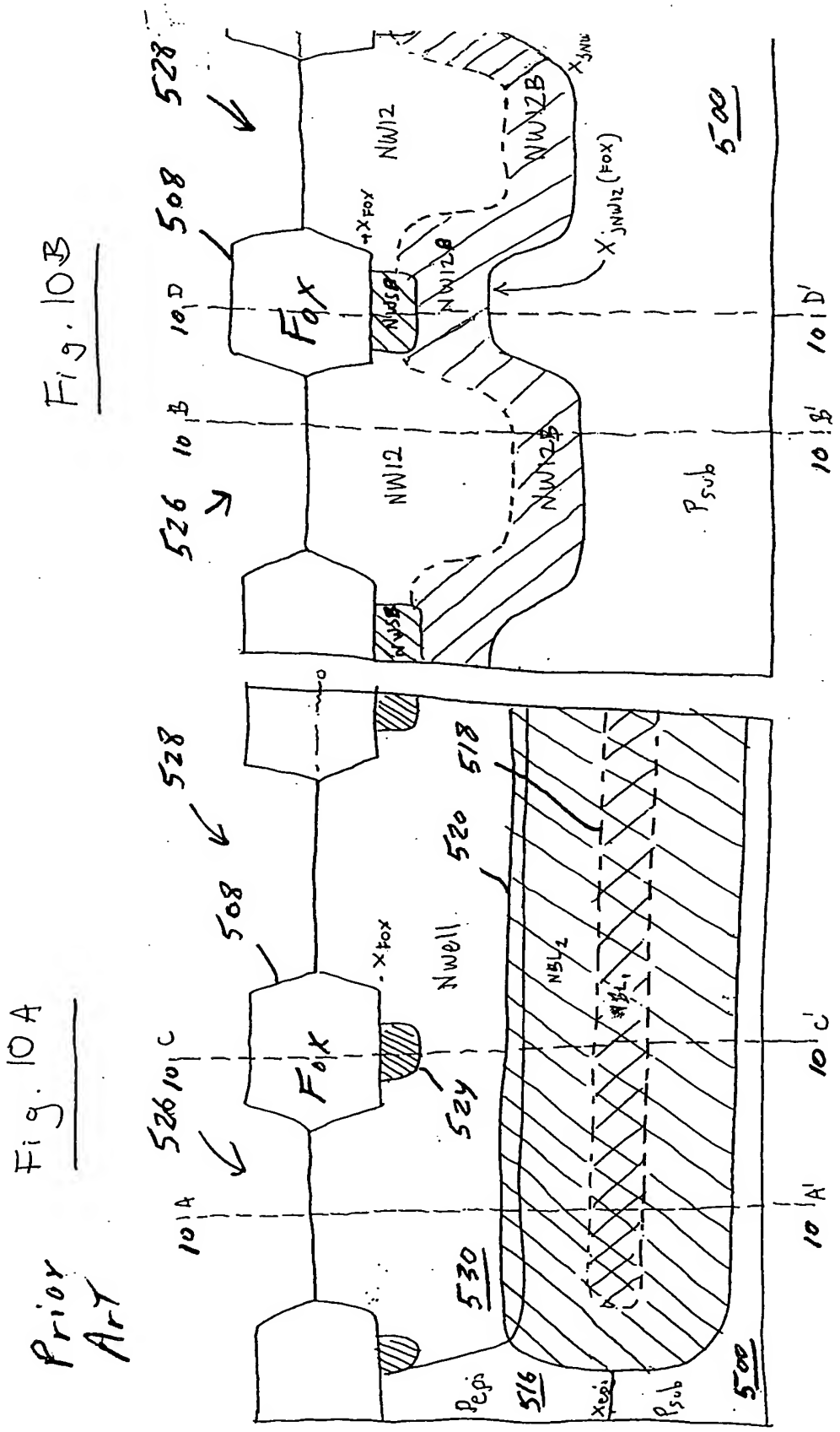

Prior Art
Fig. 10A
Fig. 10B
528
508
526
10 A
10 B
10 C
10 D
FOX
+XFOX
NW12
NW2B
XJNW12 (FOX)
XJNW
500
PSUB
A'
B'
C'
D'
518
520
NWell
NBL2
529
530
516
Xepi
Pepi

Fig. 10C

Prior Art

10A - 10A'

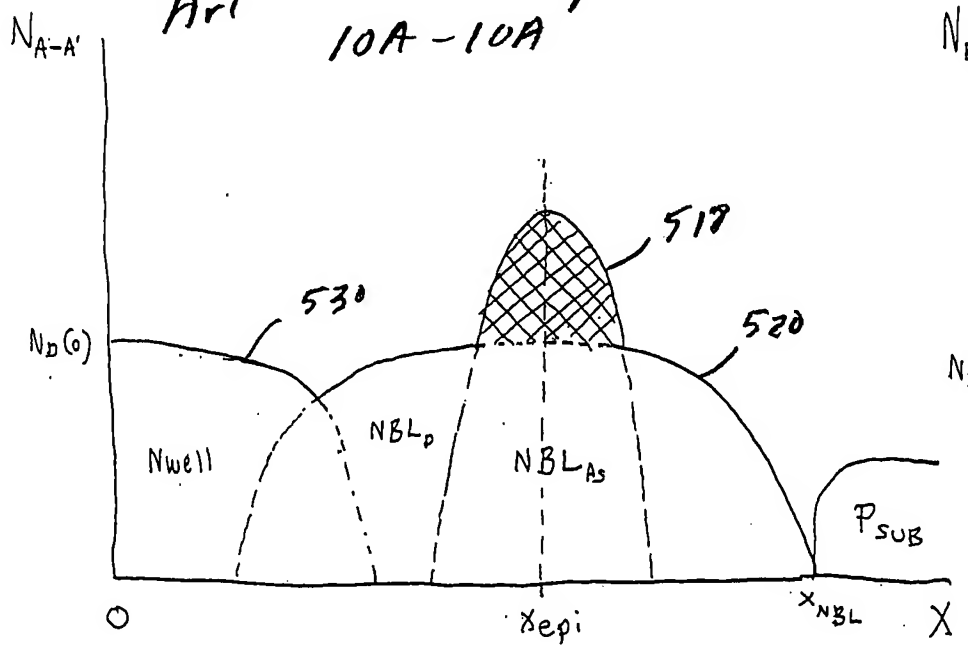
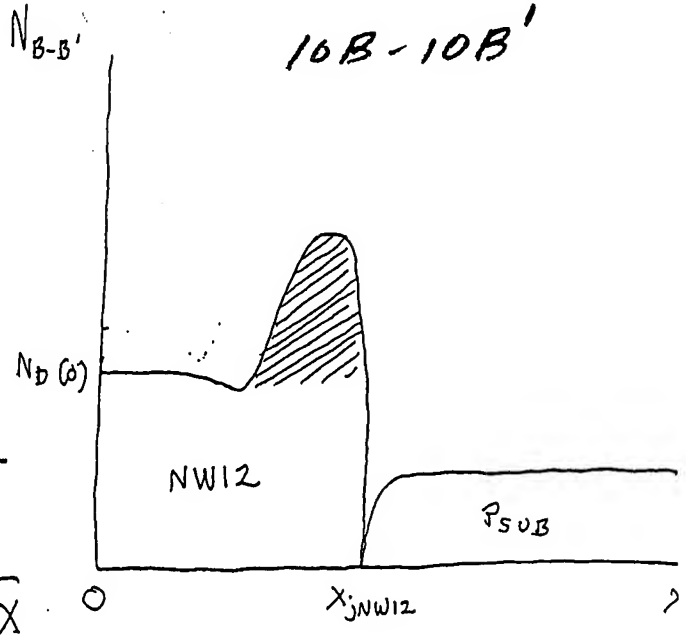


Fig. 10D

10B - 10B'



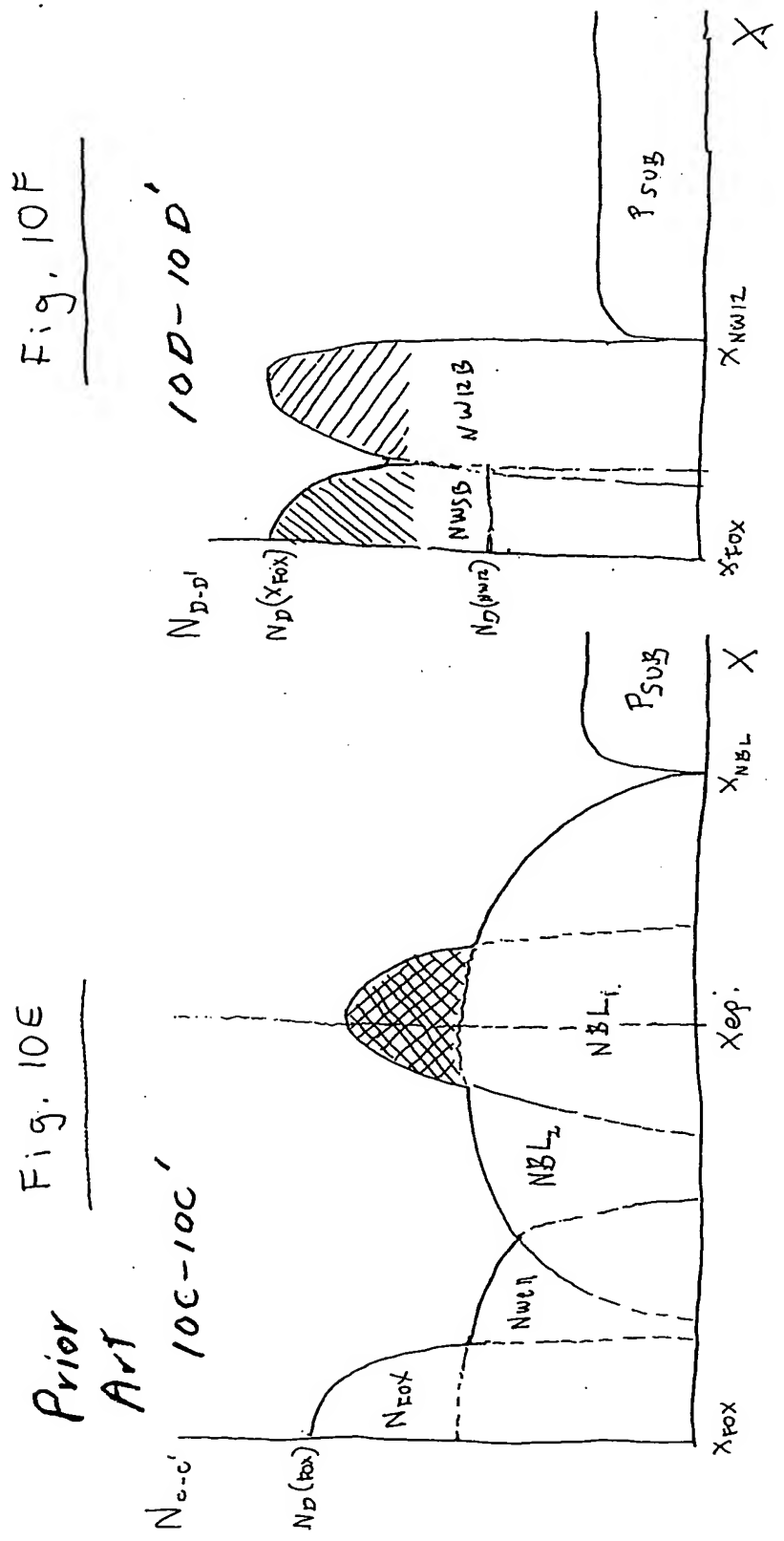

Prior Art
Fig. 10E
10C-10C'
$N_{C-C'}$
$N_D(x_{FOX})$
N_{FOX}
N_{WELL}
NBL_2
NBL_1
P_{SUB}
X_{epi}
X_{NBL}
X_{FOX}
X
Fig. 10F
10D-10D'
$N_{D-D'}$
$N_D(x_{FOX})$
$N_D(x_{NW2})$
NW2B
NW2S
P_{SUB}
X_{NW2}
X_{FOX}
X

Fig. 10G

10D-10D'

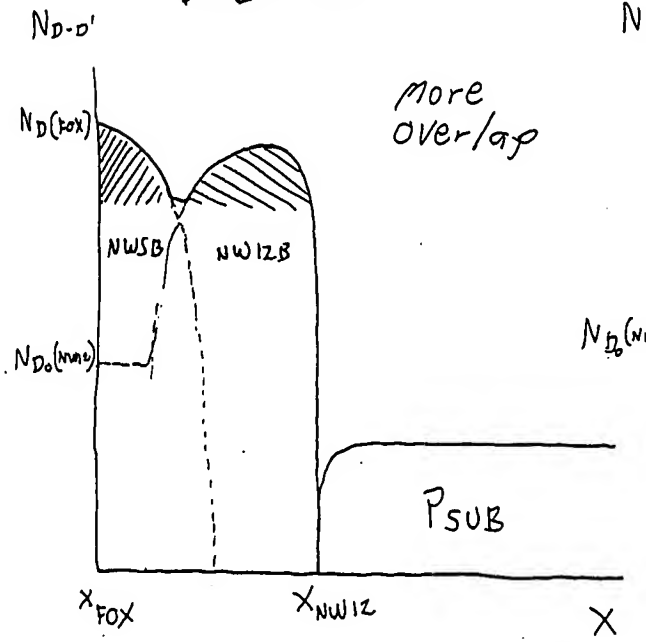


Fig. 10H

10D-10D'

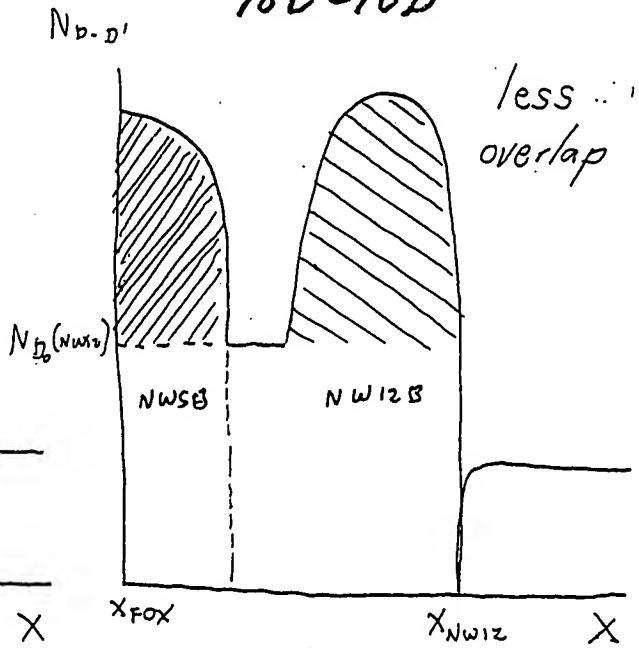
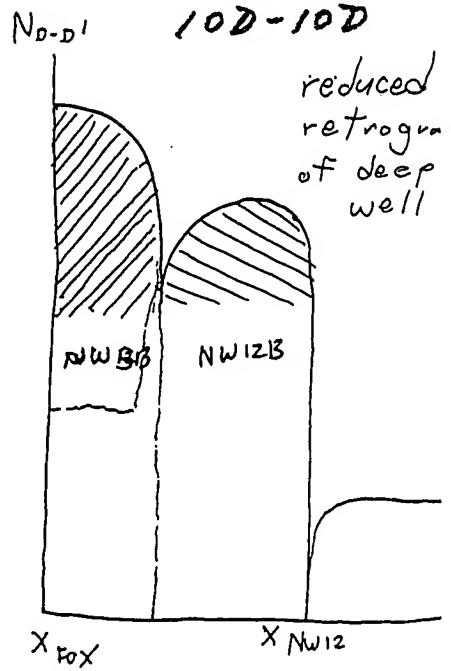


Fig. 10I

10D-10D'



27/219

Fig. 10J

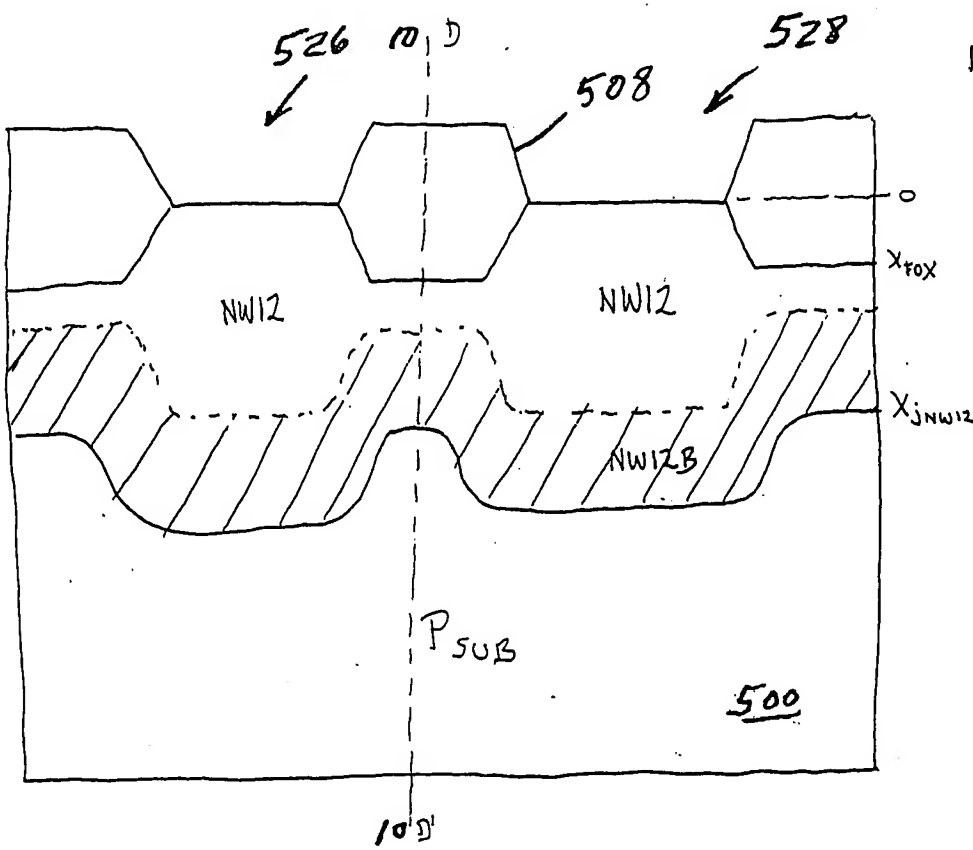
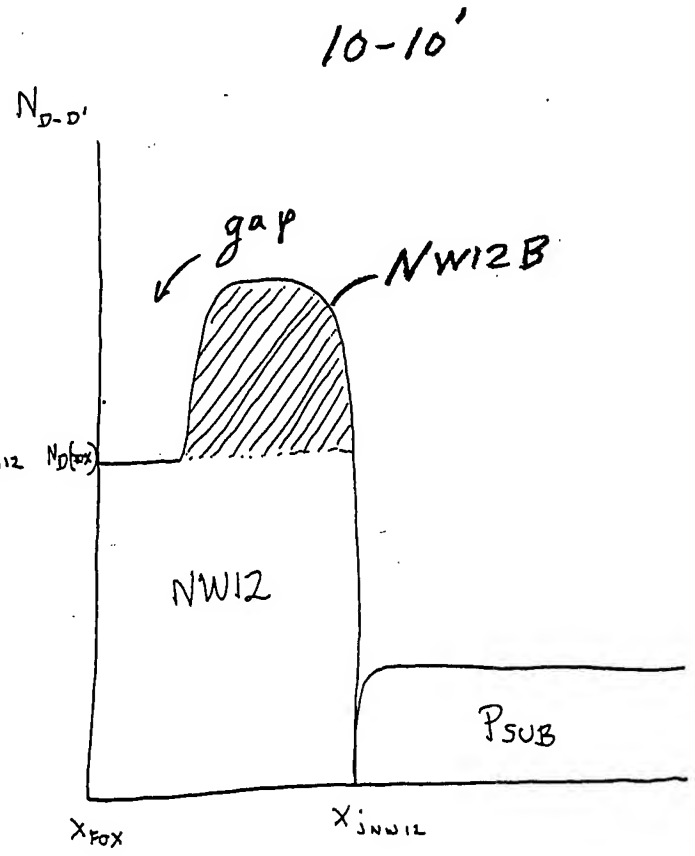


Fig. 10K



6/12/84

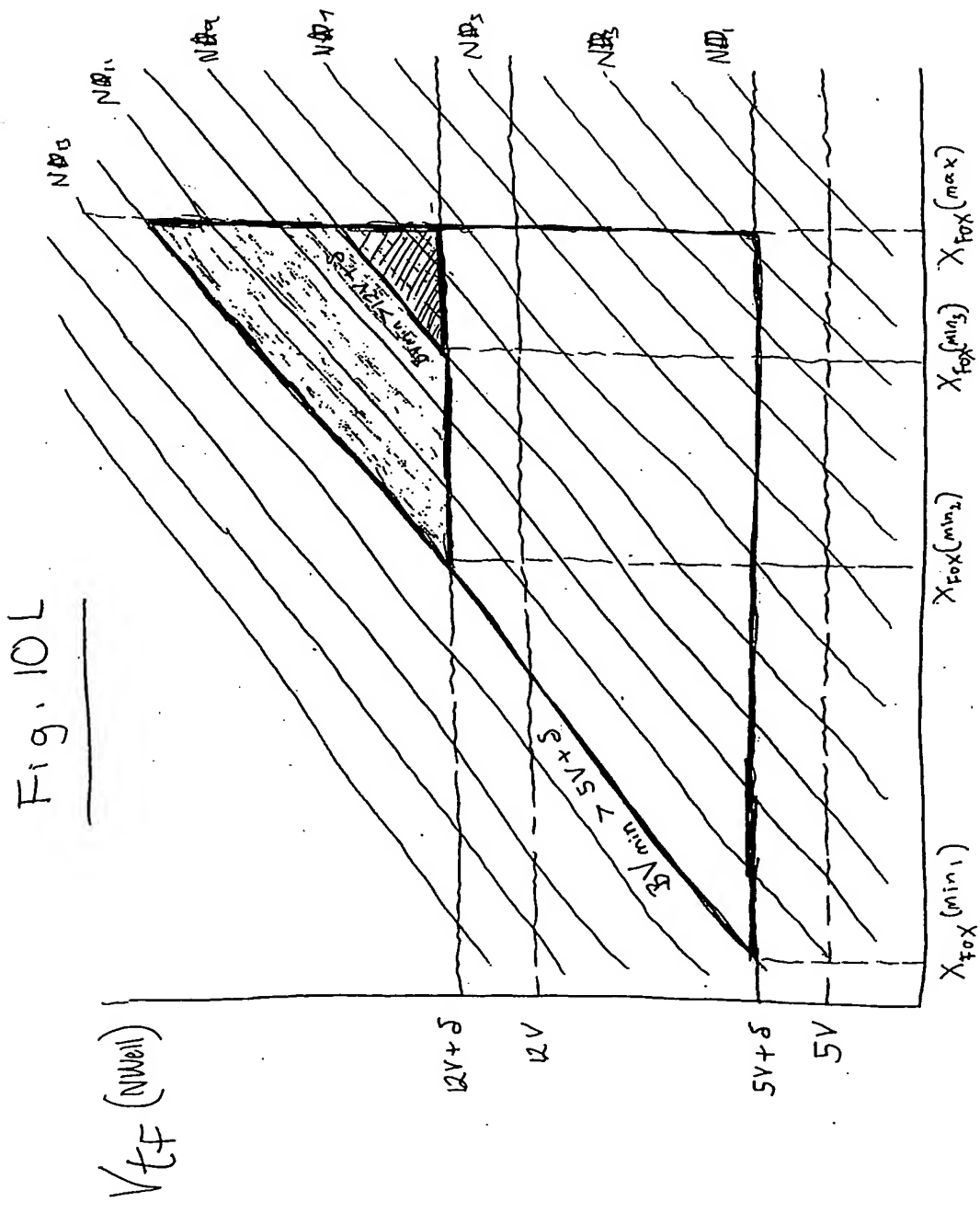

V_{tf} (NWell)
12V+δ
12V
5V+δ
5V
X_{FOX}
$X_{FOX(min_1)}$
$X_{FOX(min_2)}$
$X_{FOX(min_3)}$
$X_{FOX(max)}$
$BV_{min} > 15V+\delta$
$BV_{min} > 5V+\delta$

Fig. 10L

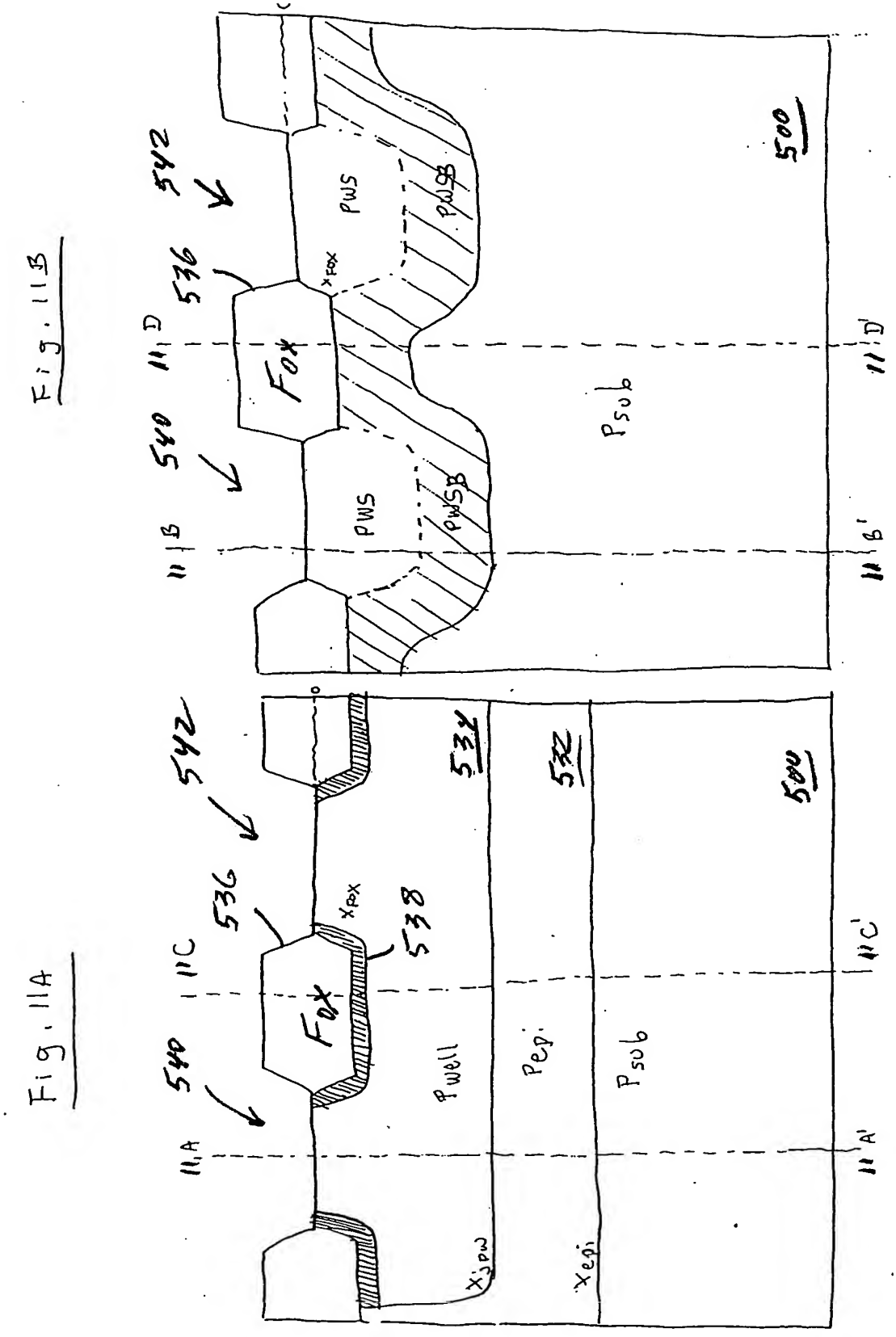


Fig. 11B
Fig. 11A
500
542
536
540
538
532
522
FOX
PWS
PWSB
Psub
Pwell
Pepi
Xjpw
Xepi
11A
11A'
11B
11B'
11C
11C'
11D
11D'

Fig. 11C

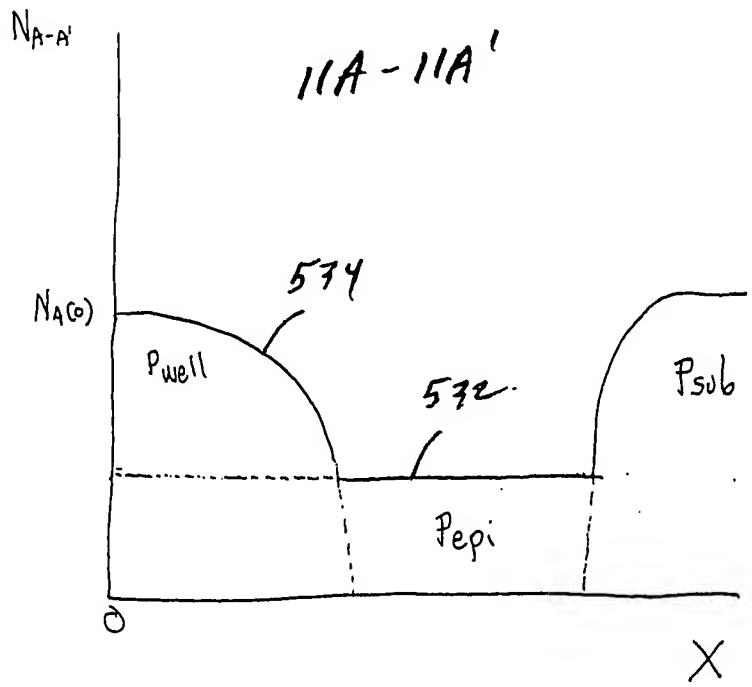


Fig. 11D

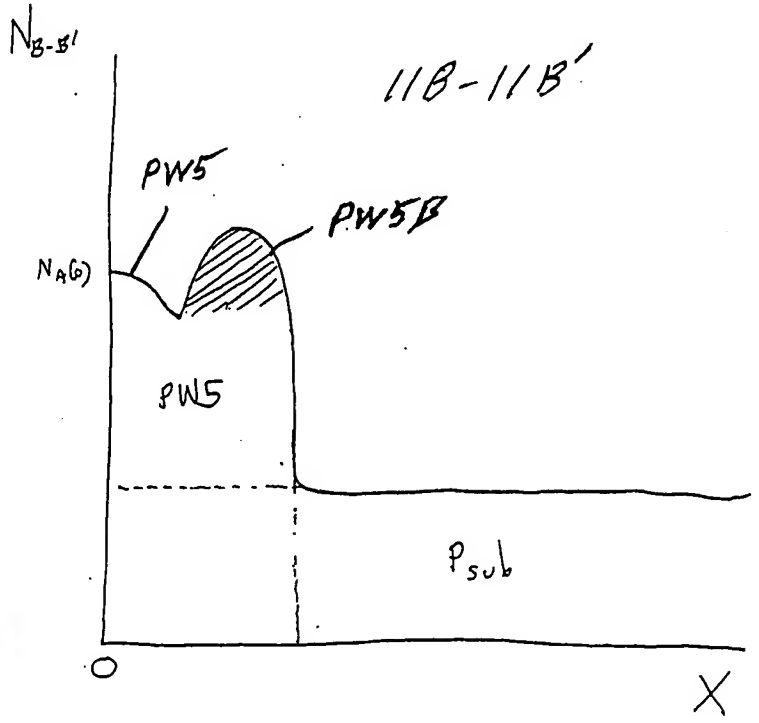


Fig. 11F

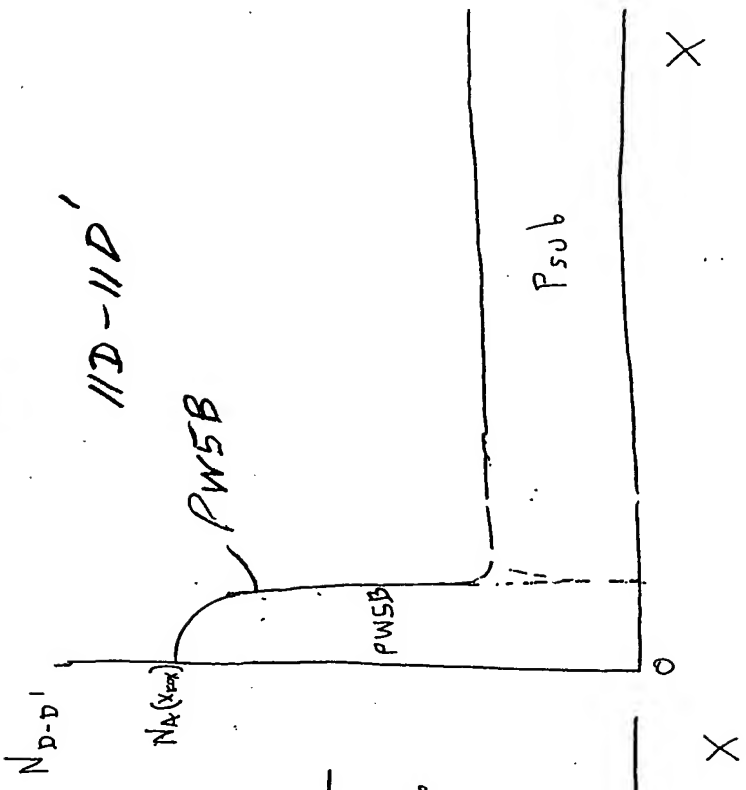


Fig. 11E

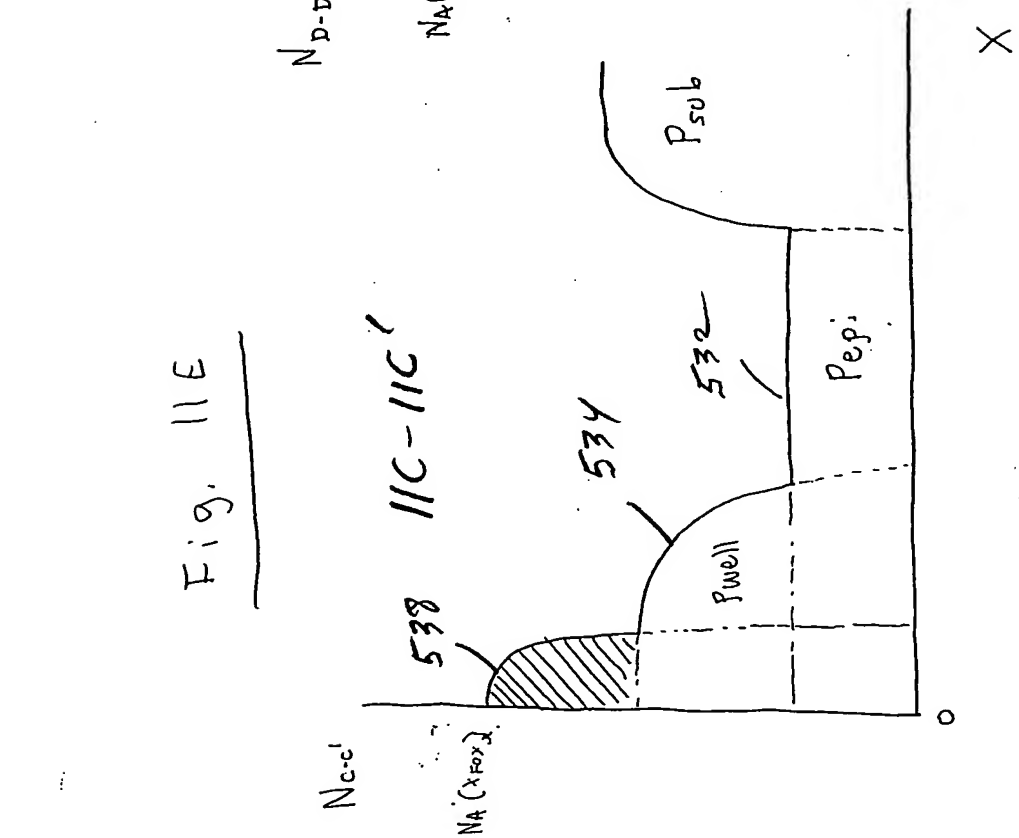


Fig. 11G

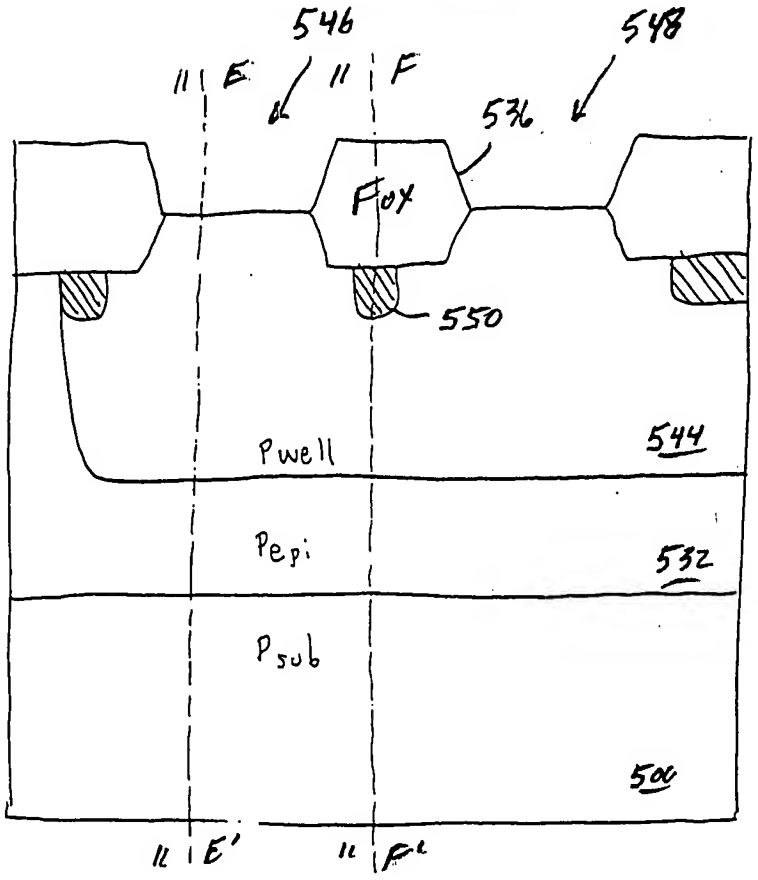


Fig. 11H

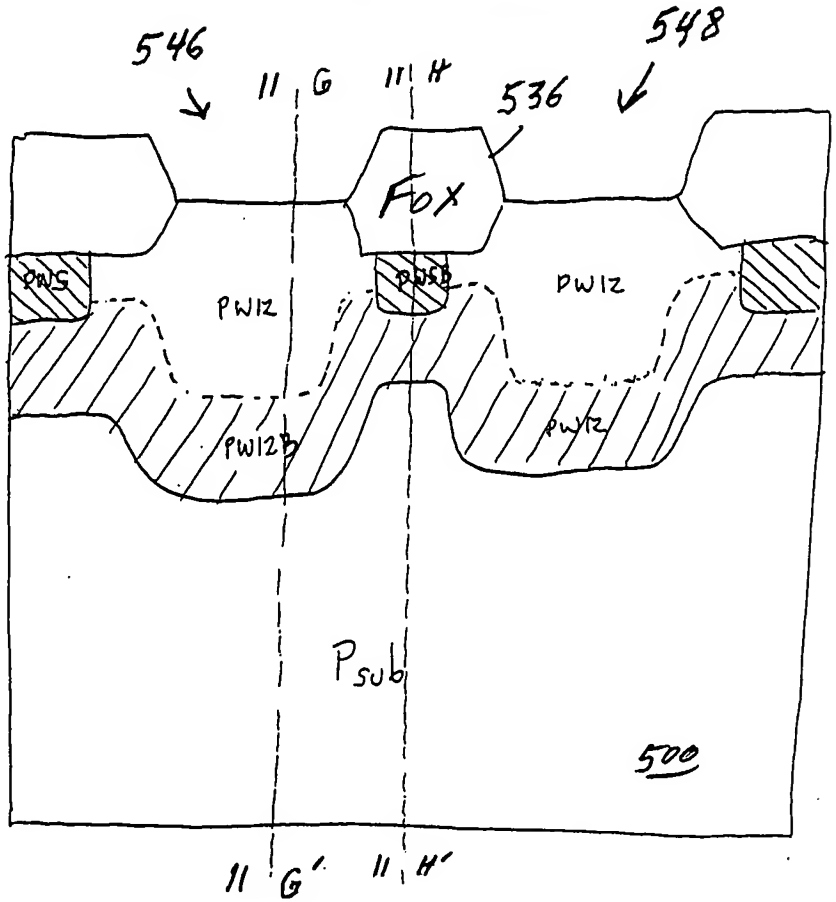


Fig. 11I

11E-11E'

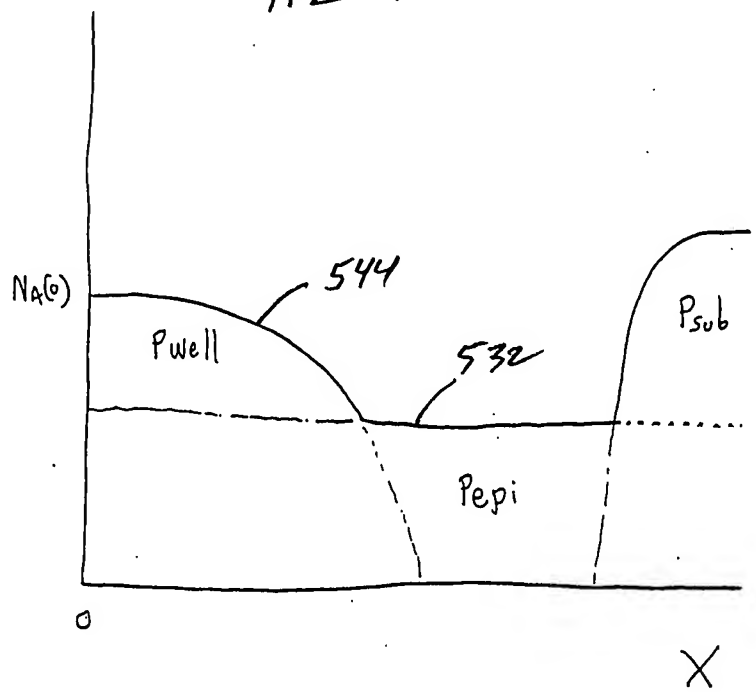


Fig. 11J

11G-11G'

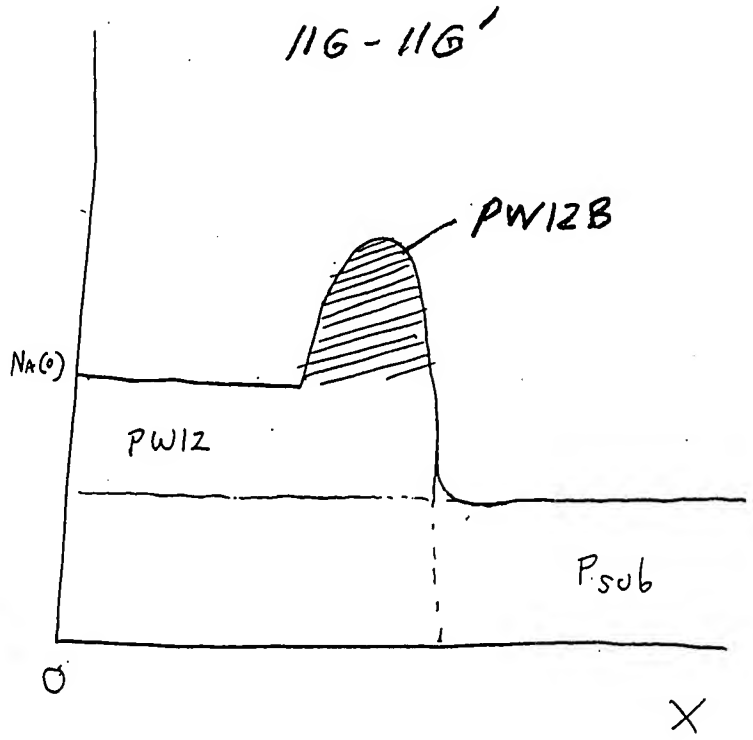


Fig. 11K

11F-11F'

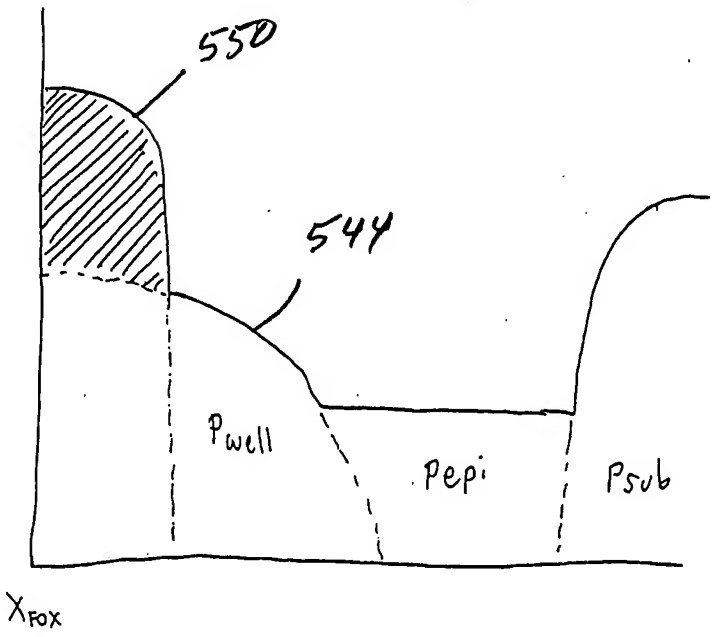


Fig. 11L

11H-11H'

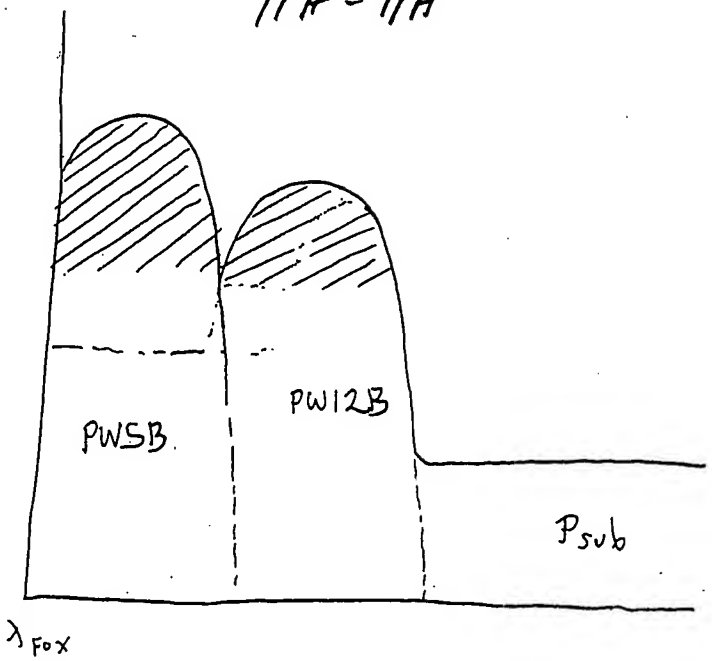


Fig. 12A

epitaxial

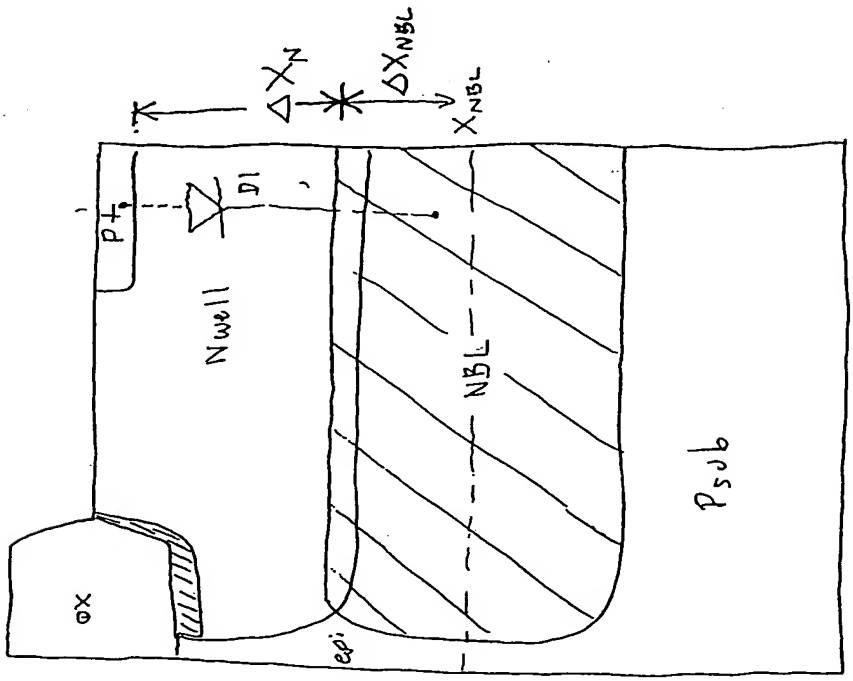


Fig. 12B

implanted

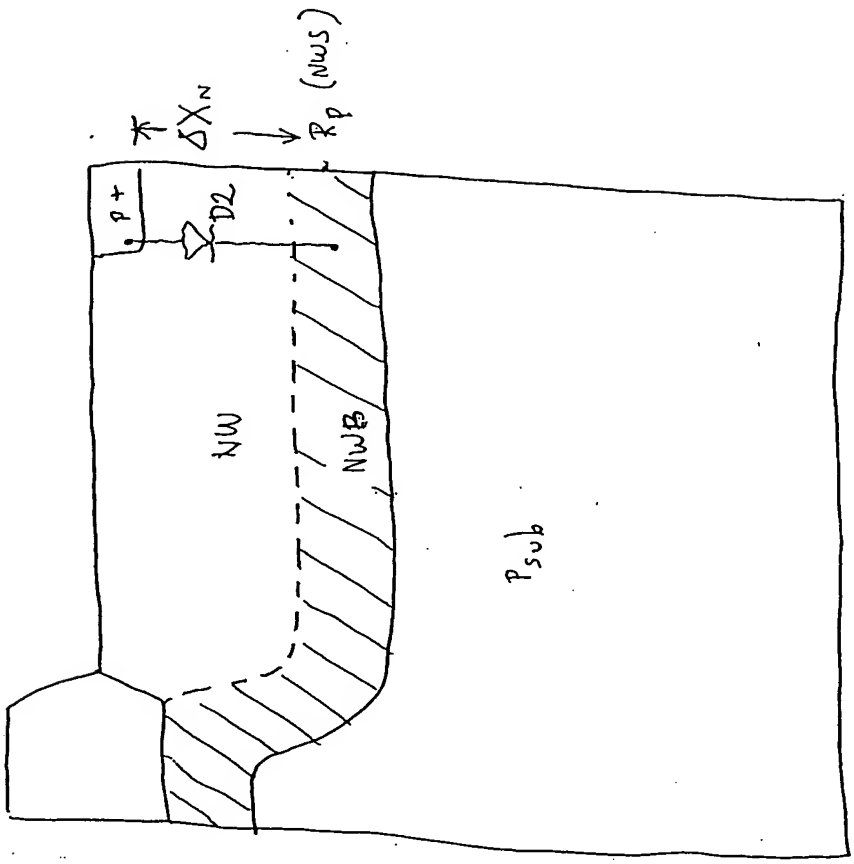


Fig. 12C

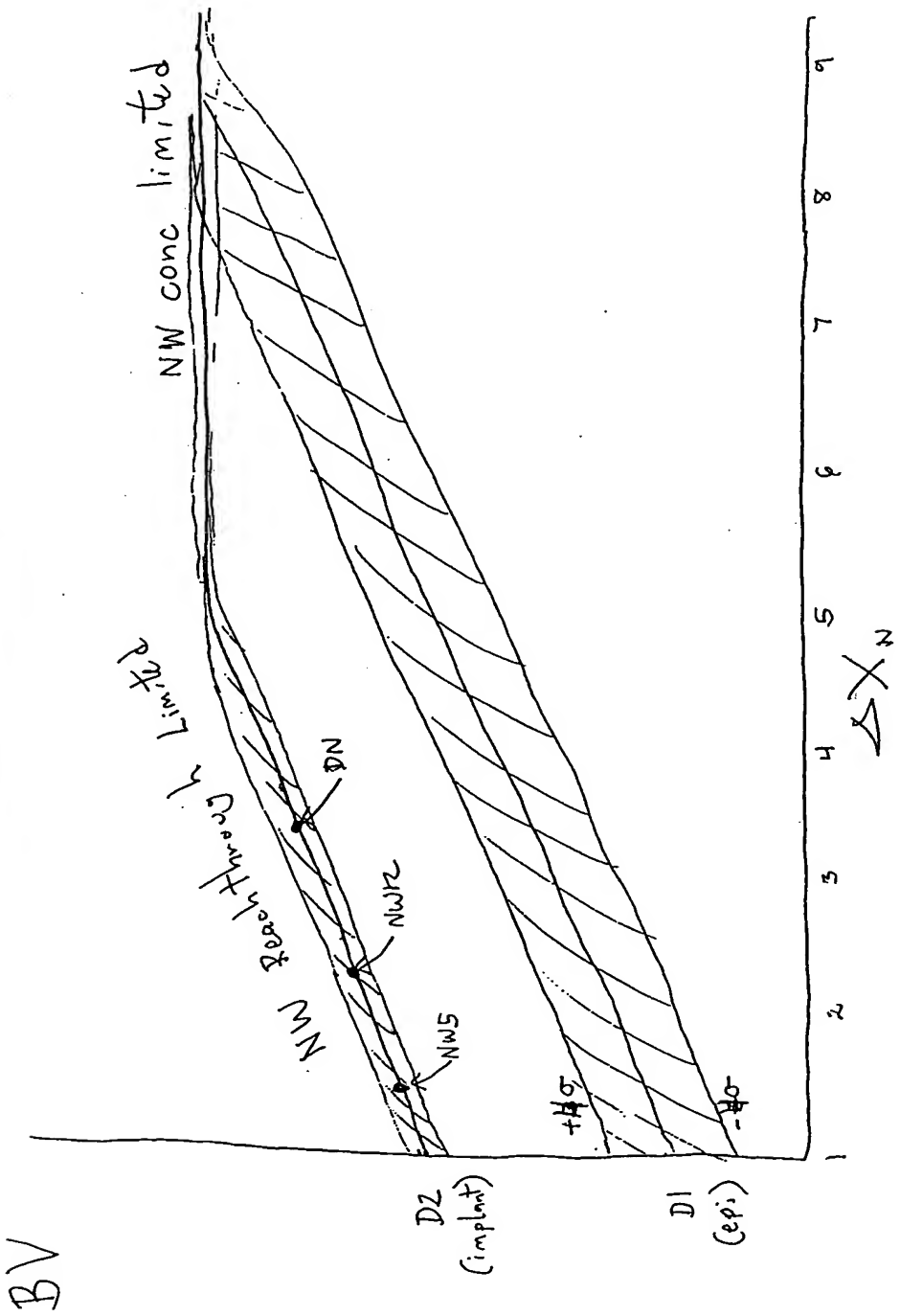

BV
D2
(implant)
D1
(epi)
NW punch through limited
NW conc limited
DN
NW2
NW5
+Hσ
-Hσ
1
2
3
4
5
6
7
8
9
N
X

Fig. 13A

Prior Art

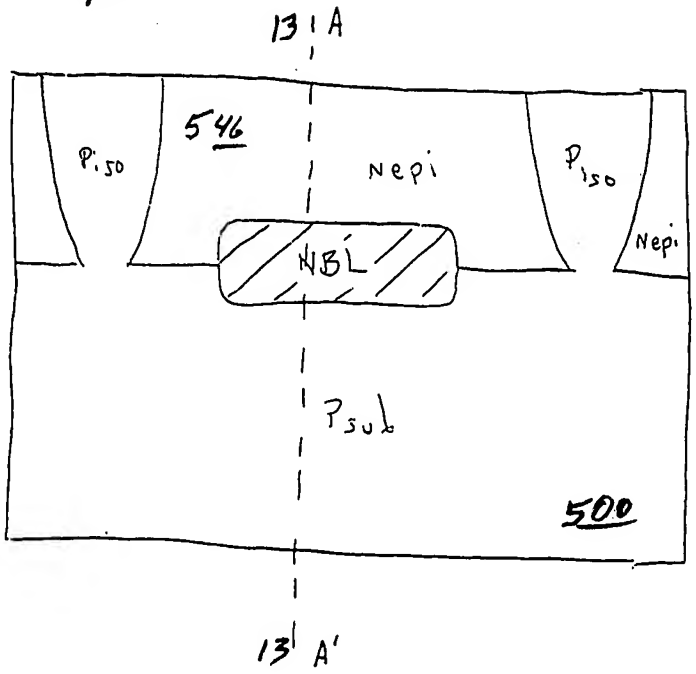


Fig. 13B

Prior Art

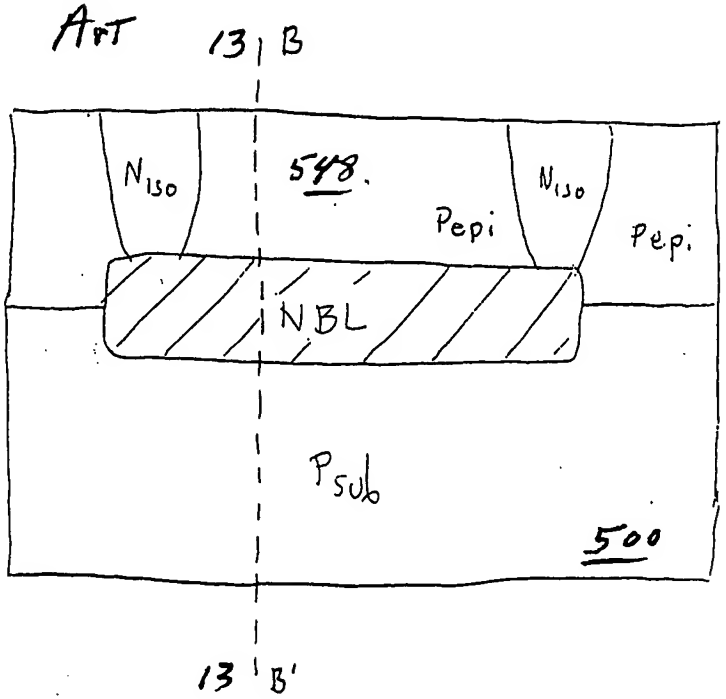


Fig 13C

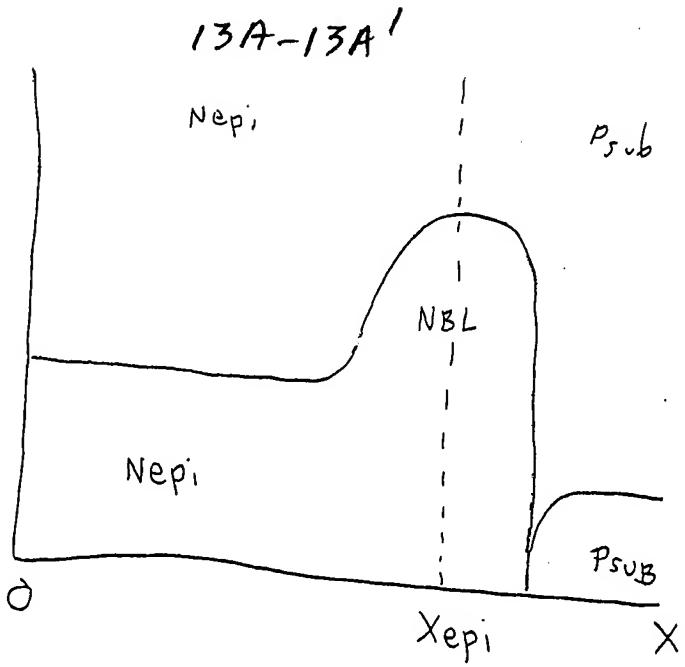


Fig 13D

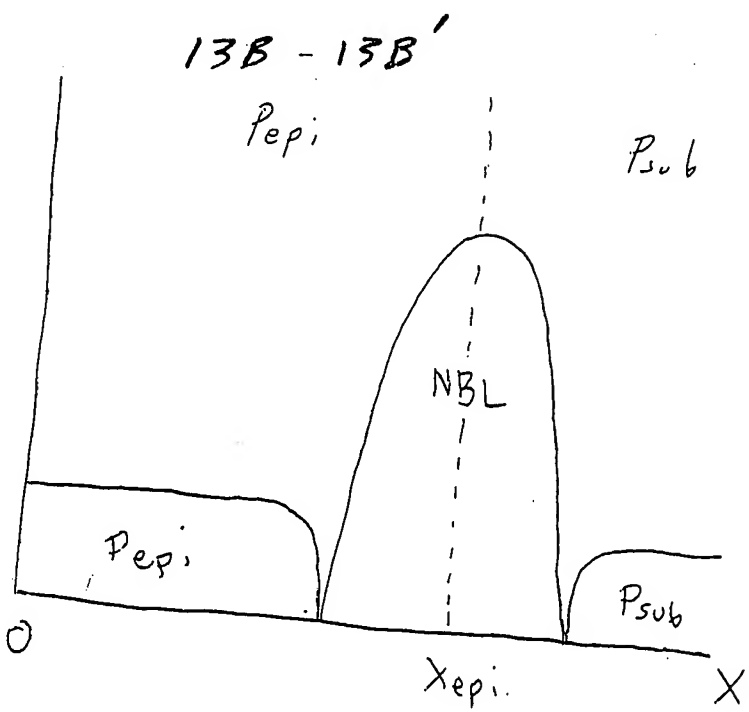


Fig. 13H

13D-13D'

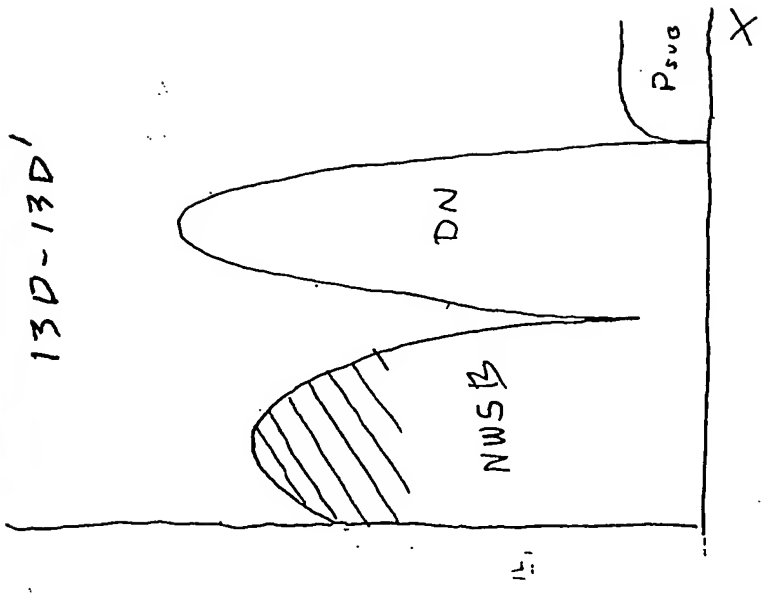
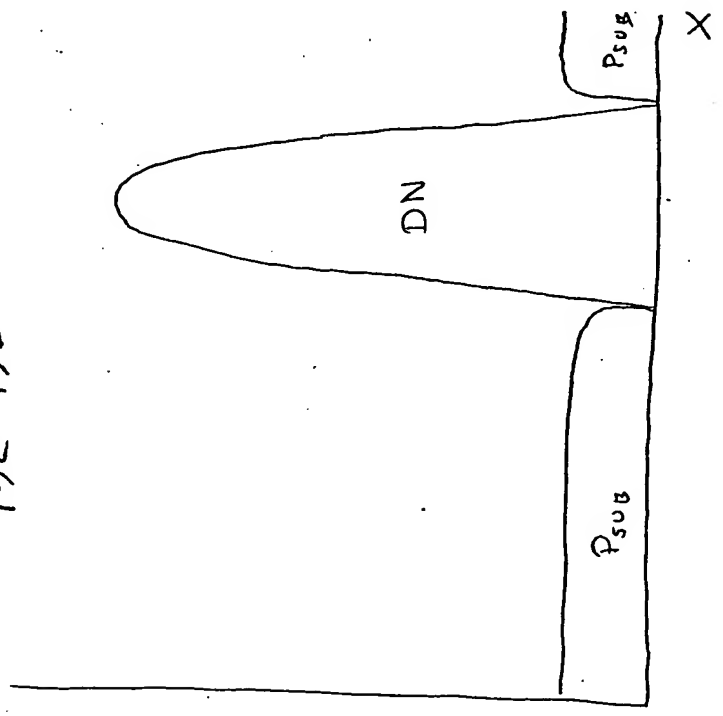


Fig. 13G

13C-13C'



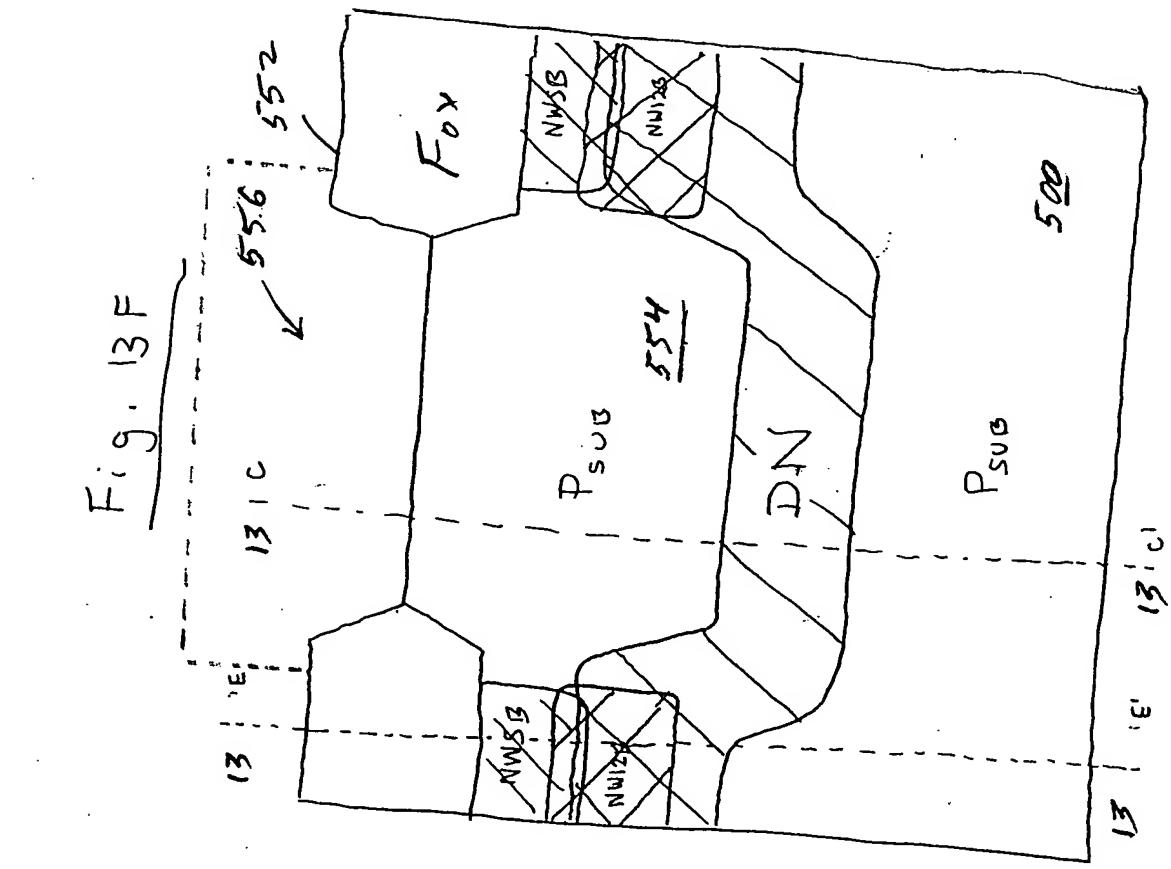


Fig. 13F
552
556
554
500
F_{OX}
NWSB
NWIM
P_{SUB}
DN
P_{SUB}
13
13'
13 E
13 E'
13 C
13 C'

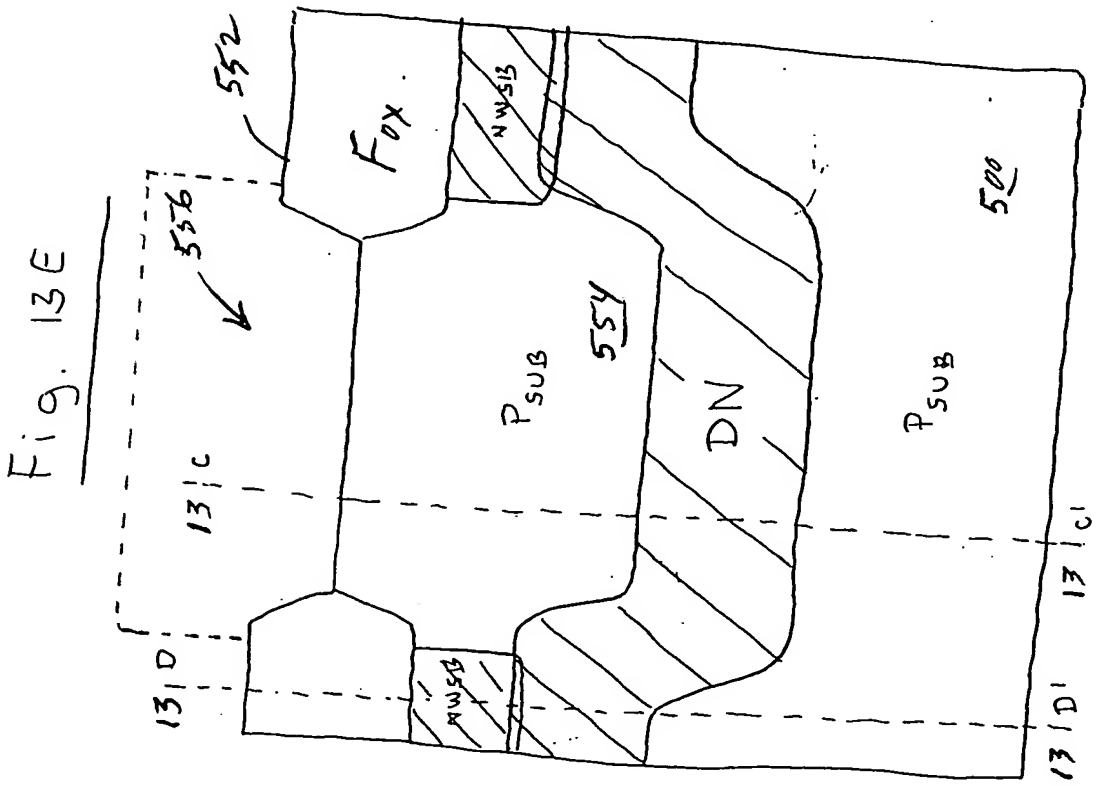
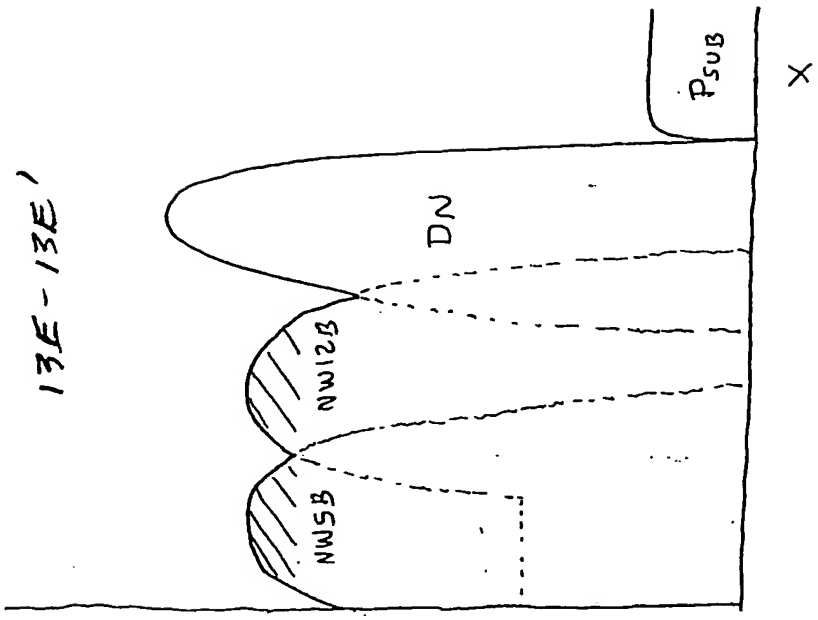


Fig. 13E
552
556
554
500
F_{OX}
NWSB
P_{SUB}
DN
P_{SUB}
13 C
13 C'
13 D
13 D'

Fig. 13I

13E - 13E'



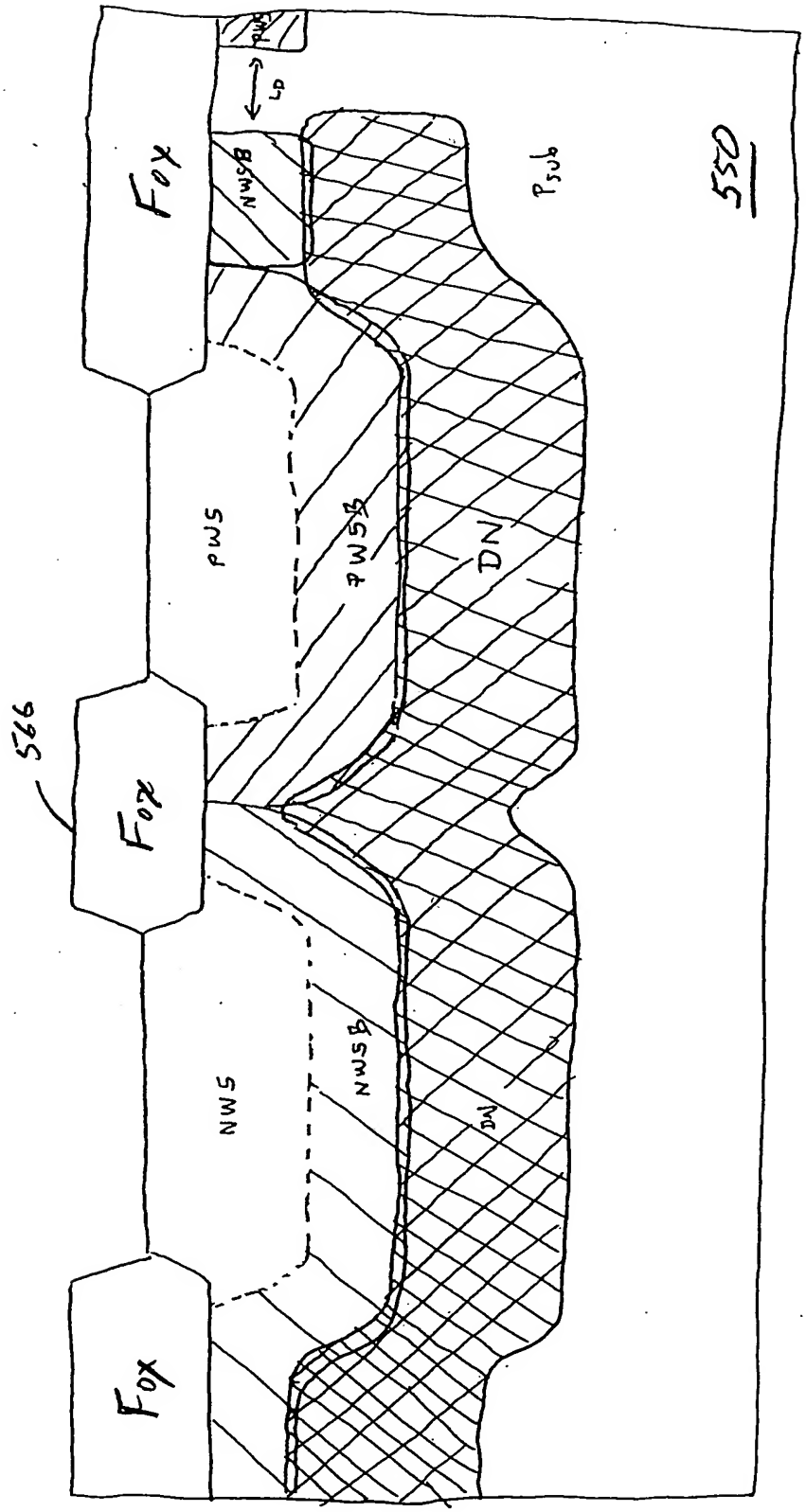


Fig 14A

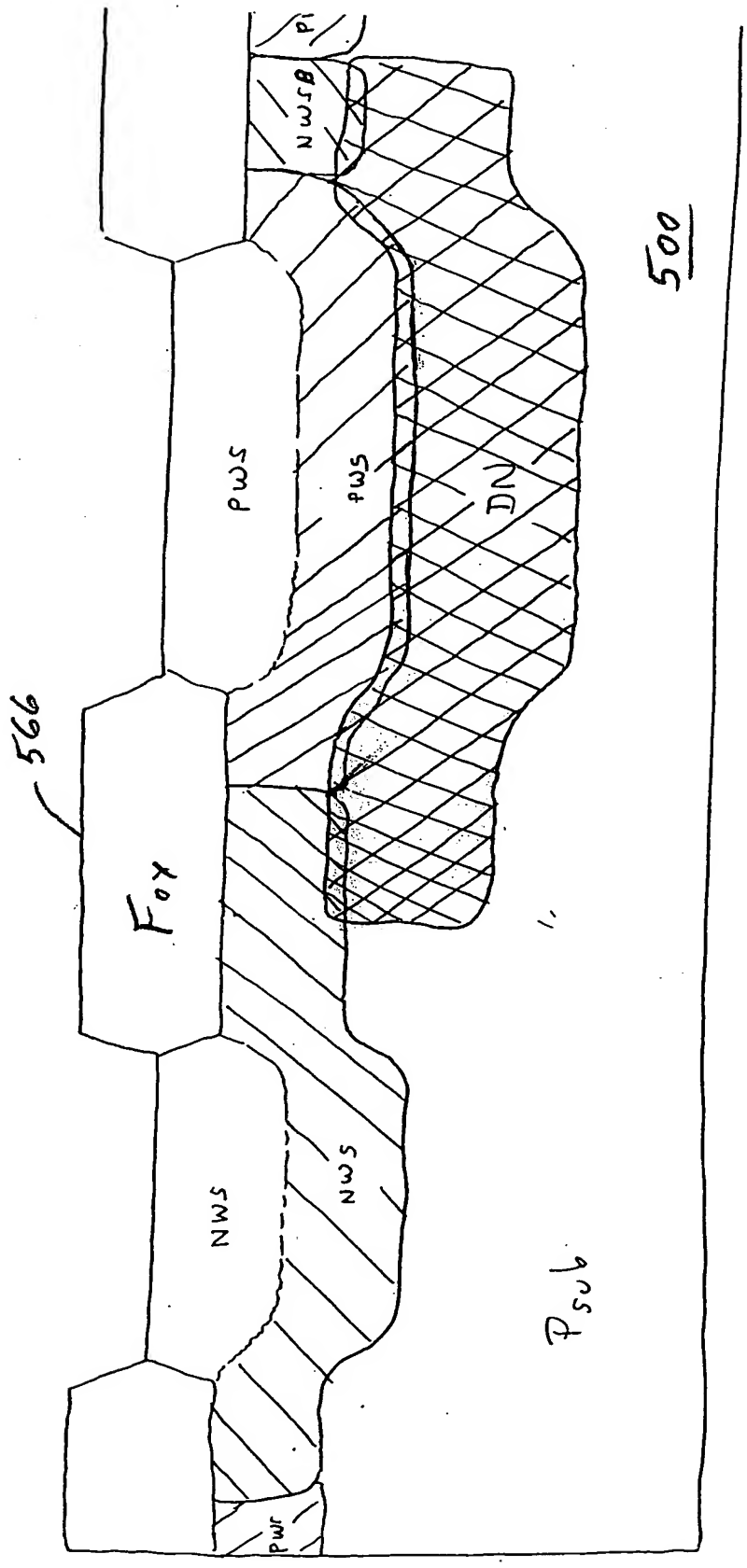


Fig. 14B

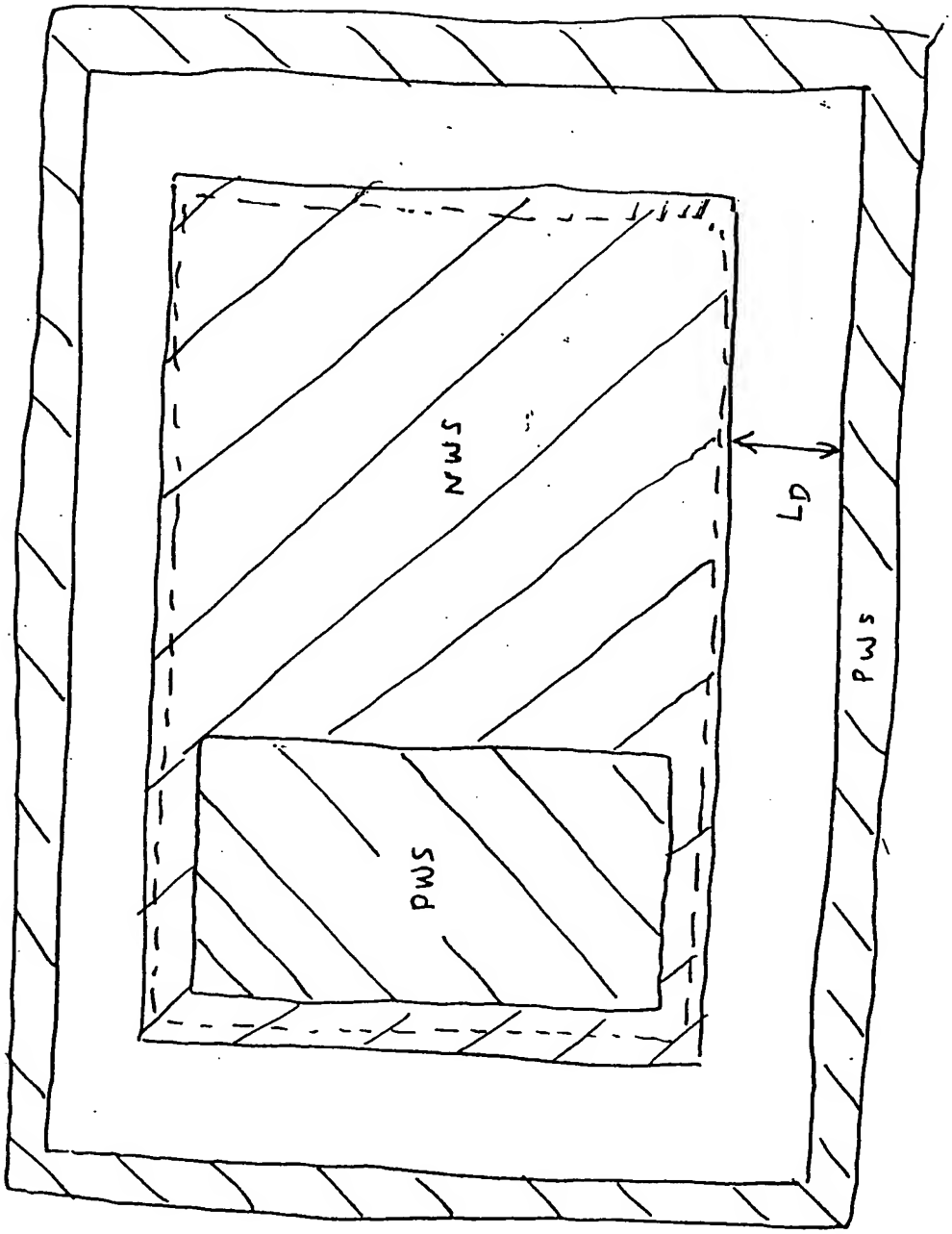


Fig. 14C

Fig. 14E

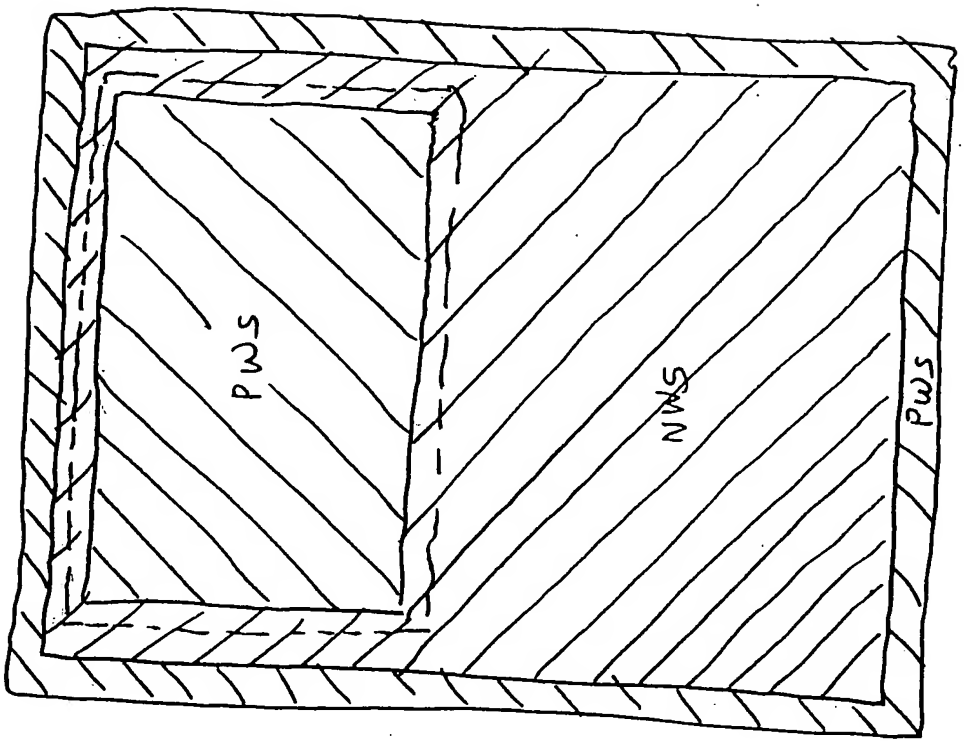
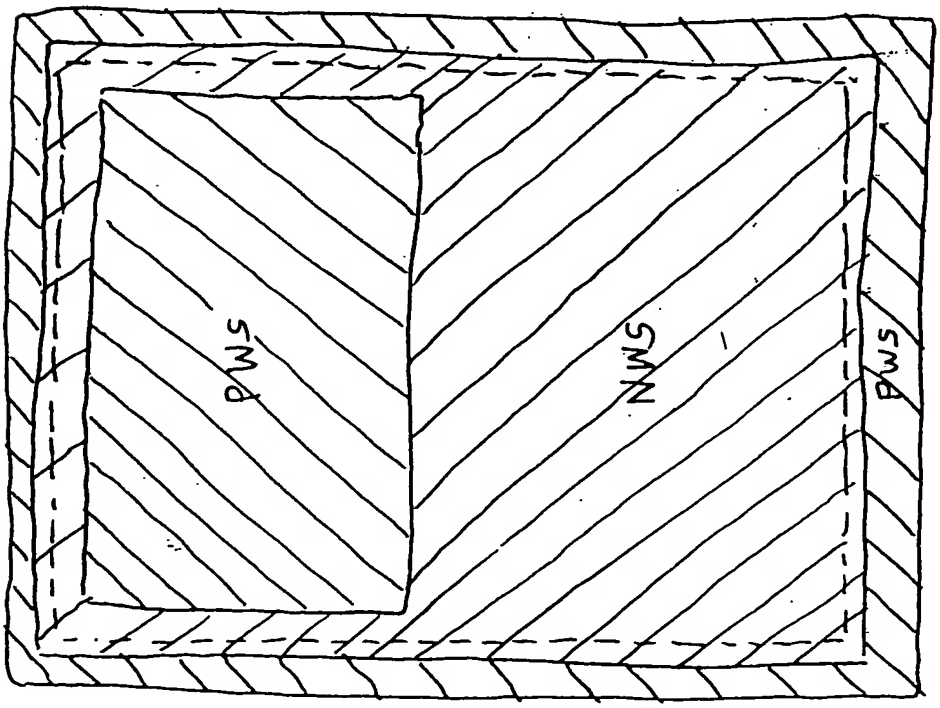


Fig 14D



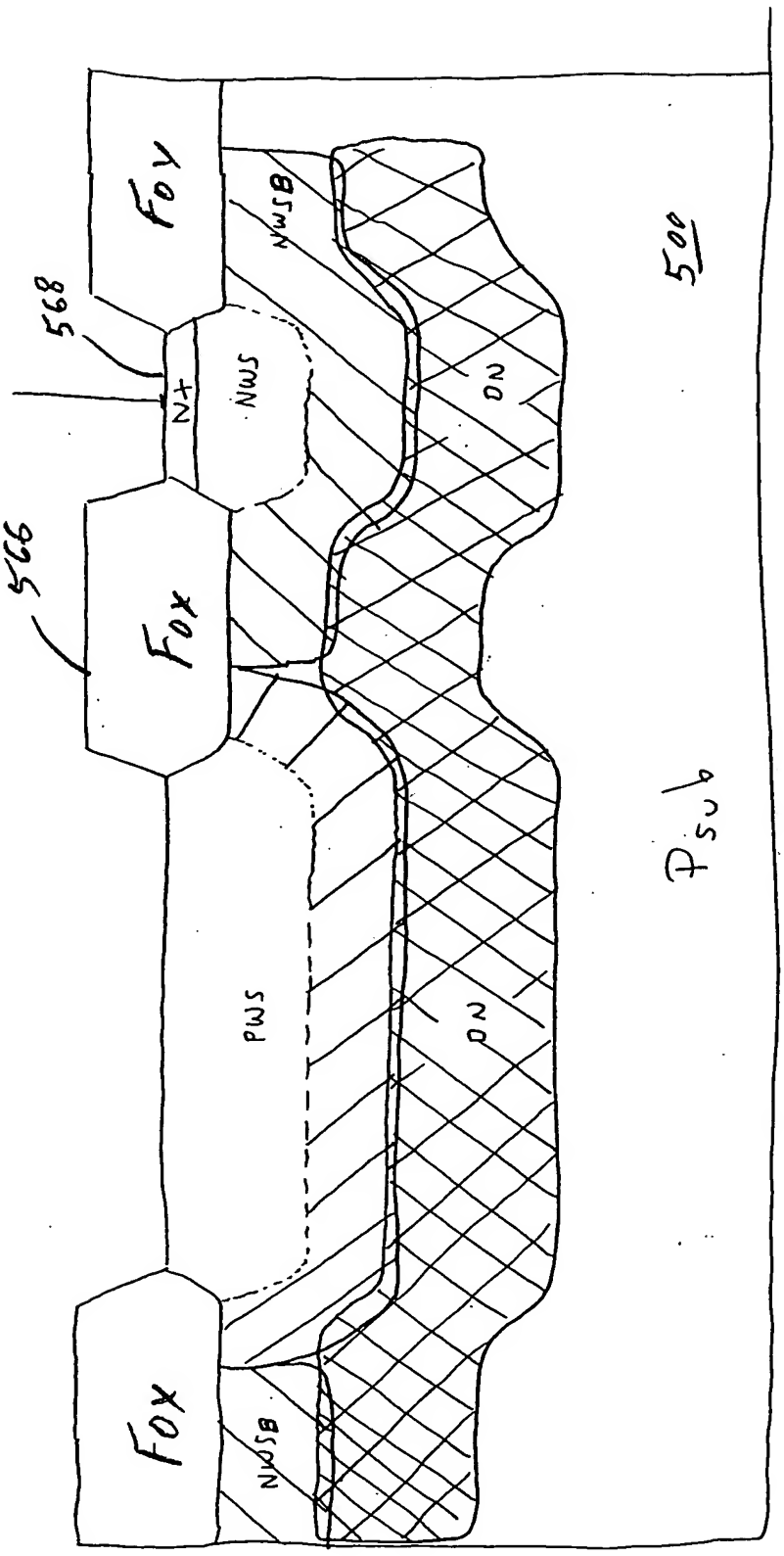

FOX
FOX
FOX
568
566
isolation
N+
NWS
NWSB
DN
PWS
DN
NWSB
500
Psub

Fig. 14F

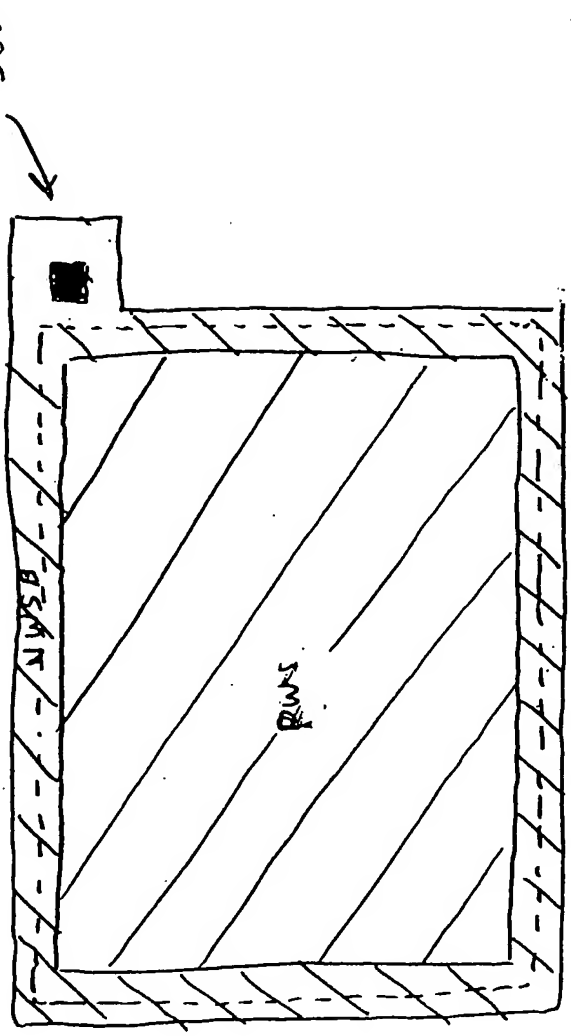


Fig. 146

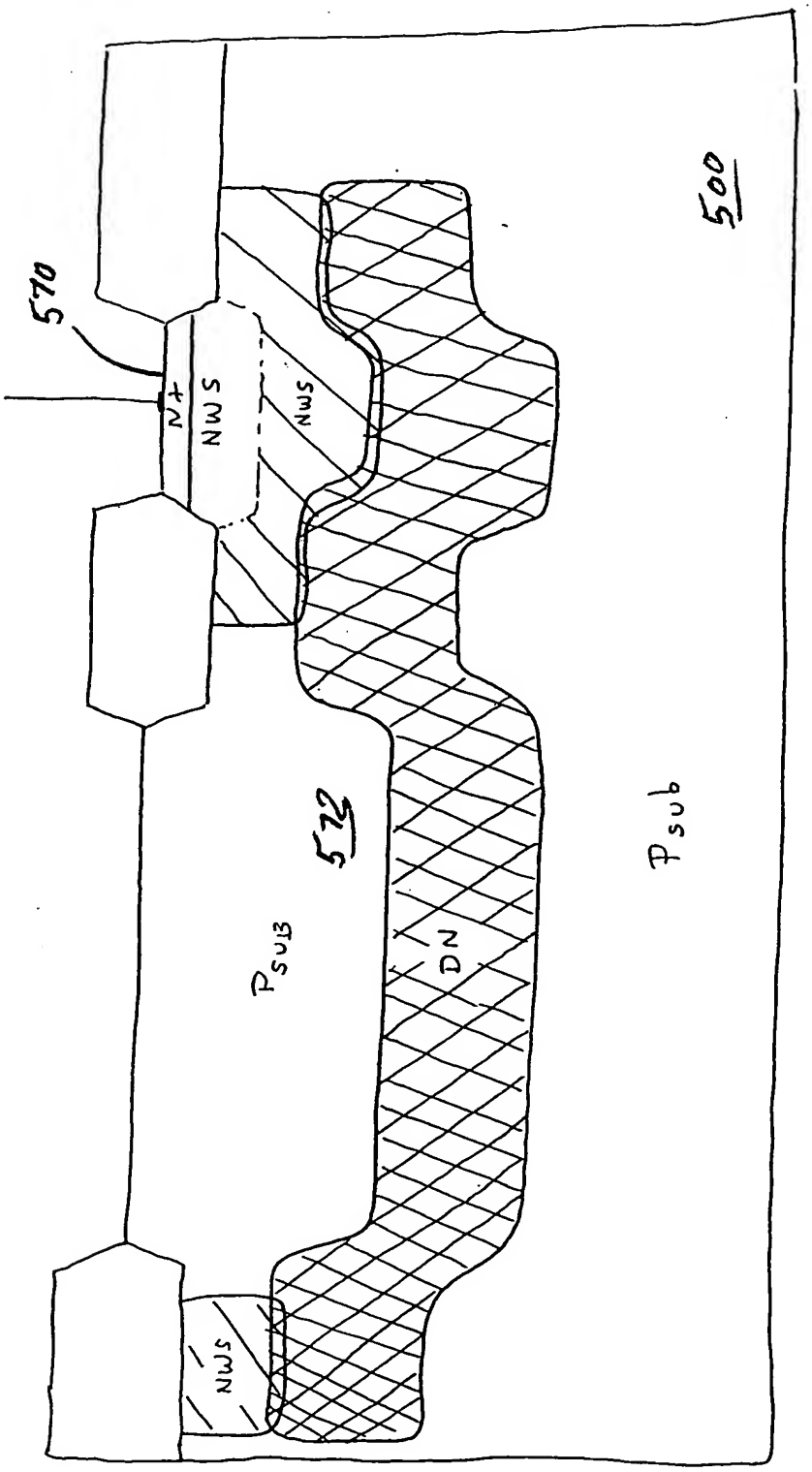


Fig. 14H

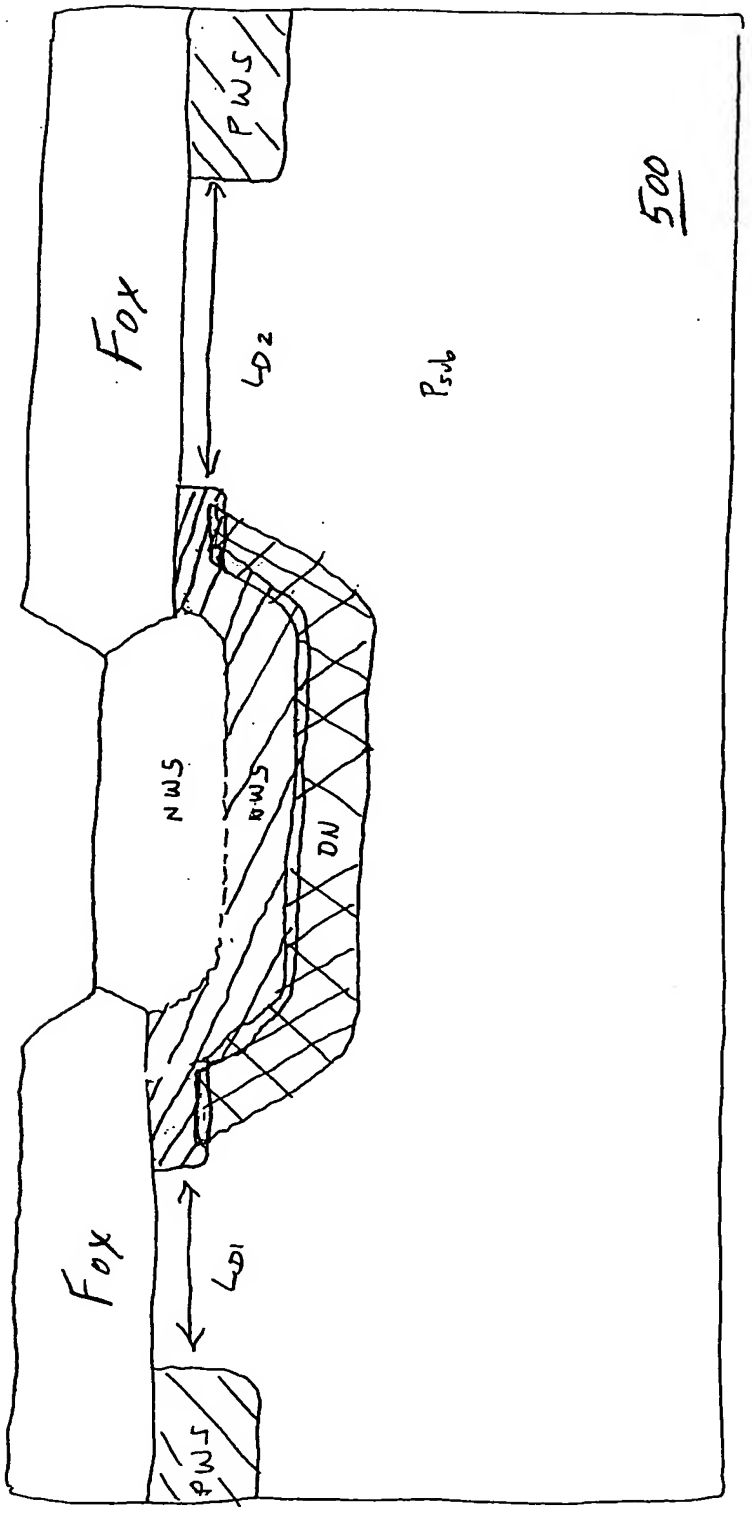


Fig. 14I

Fig. 143

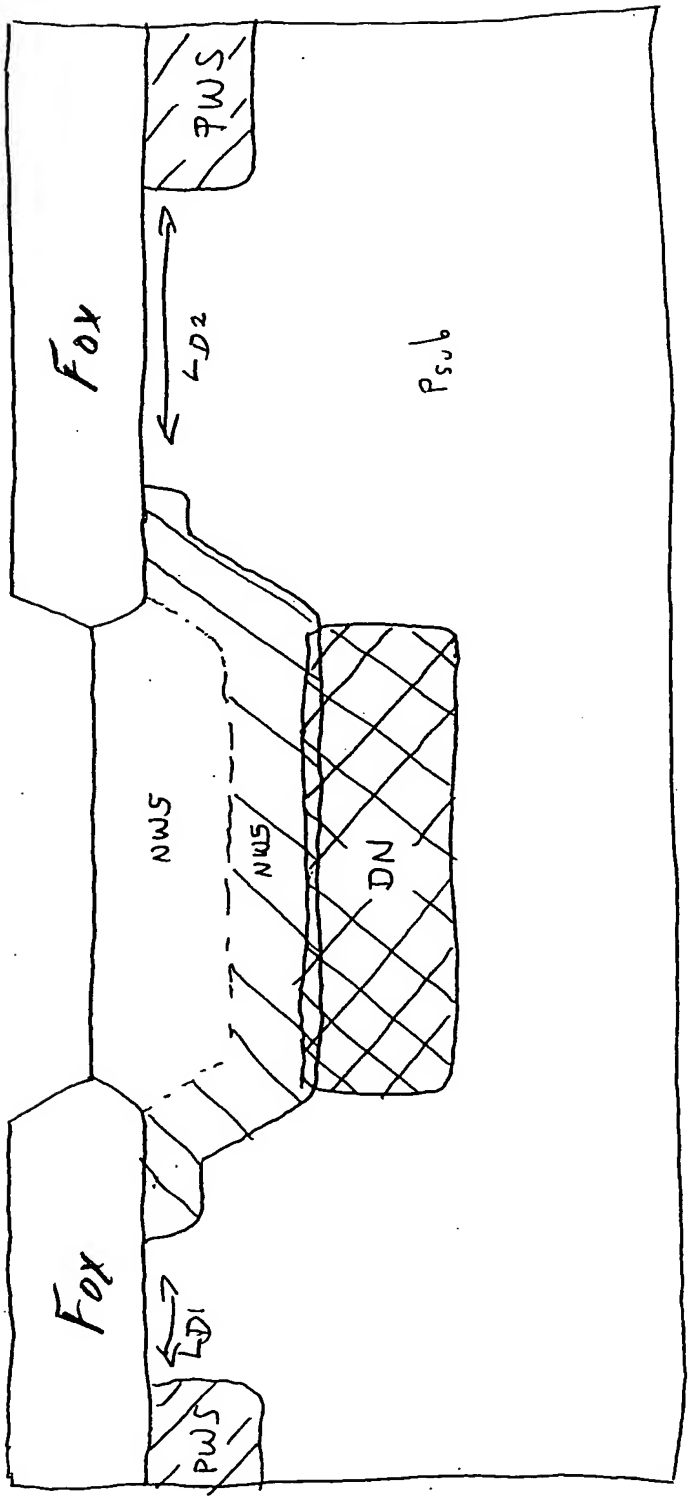


Fig. 14K

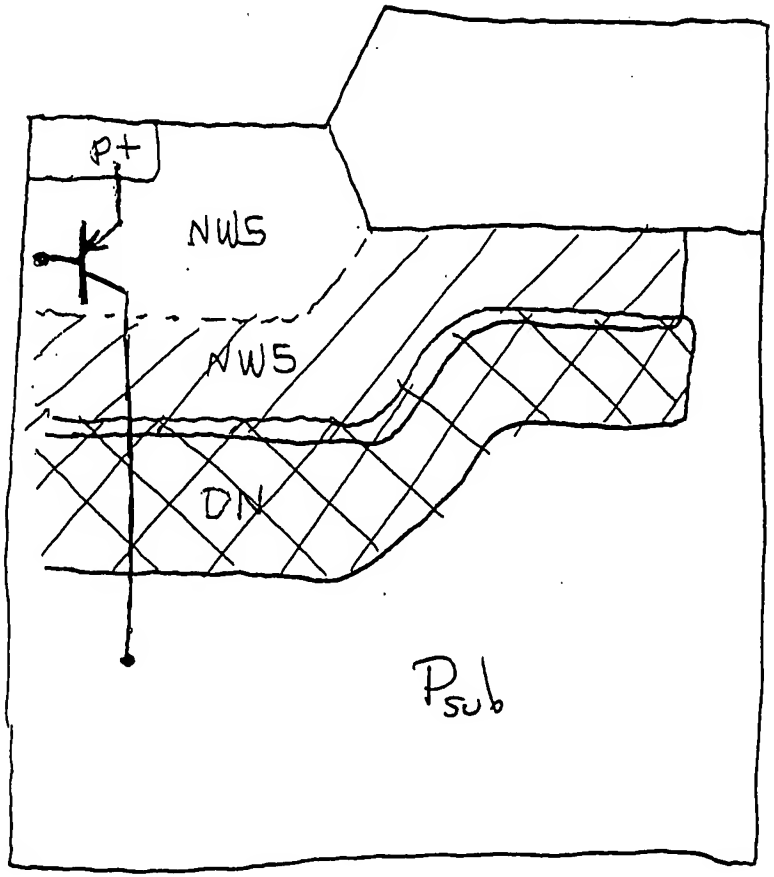
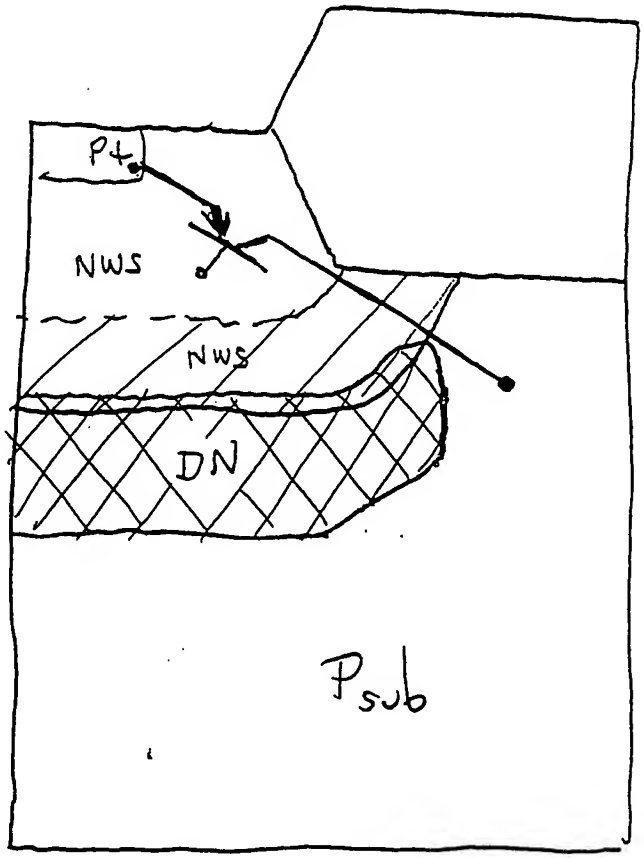


Fig. 14L



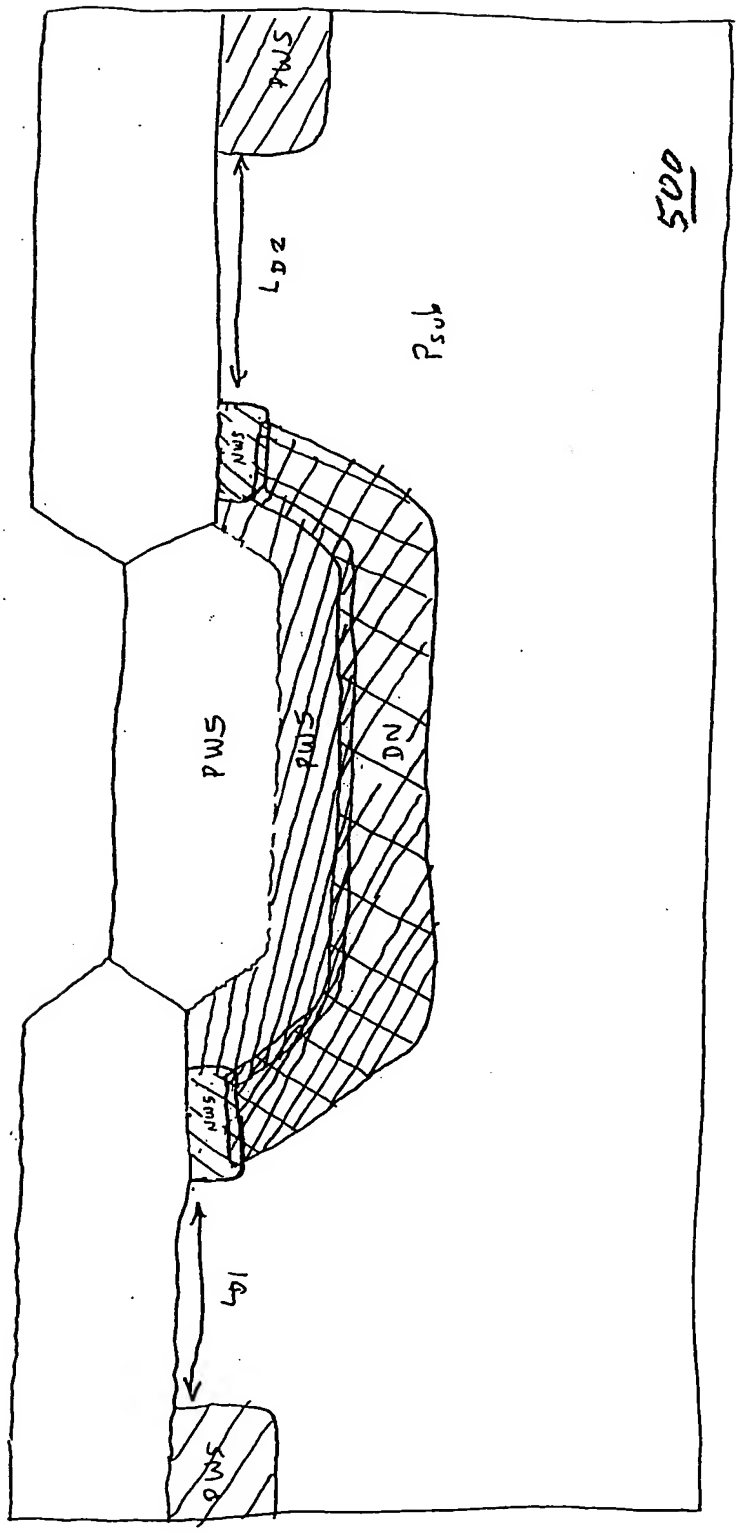


Fig. 14M

Fig. 14N

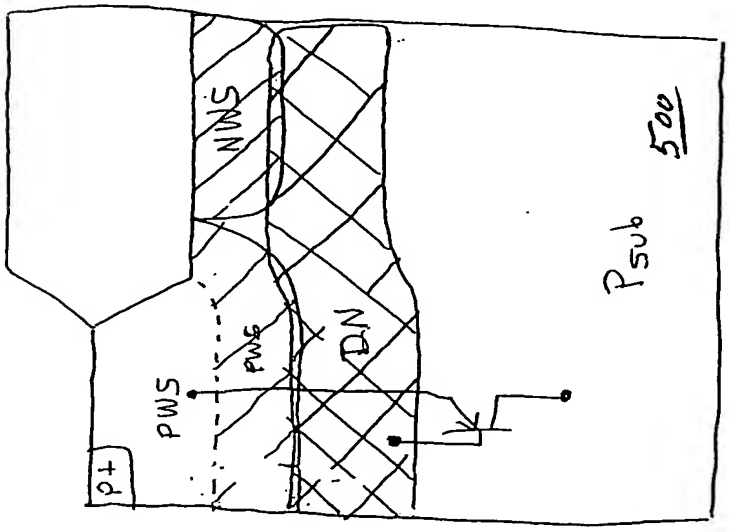


Fig. 14O

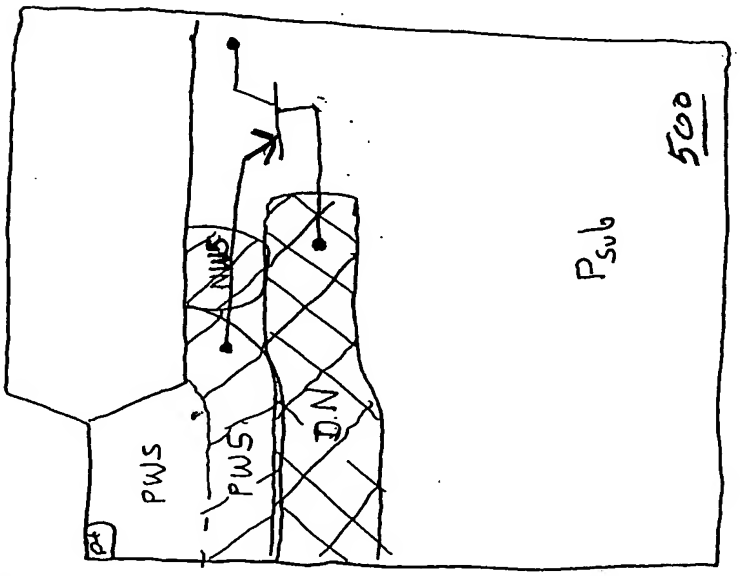


Fig. 14P

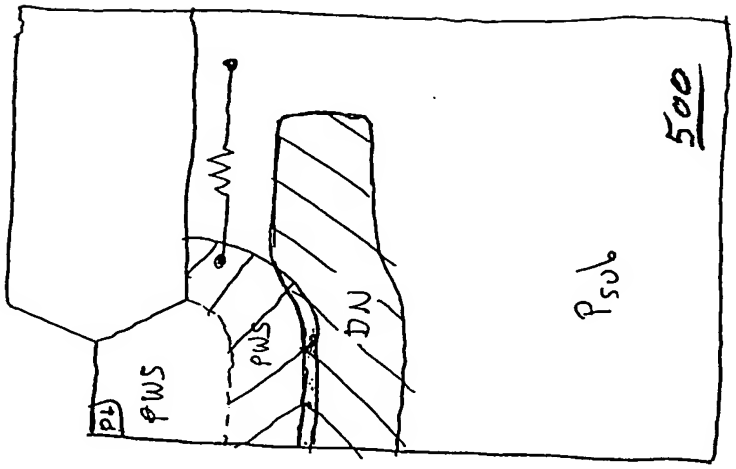
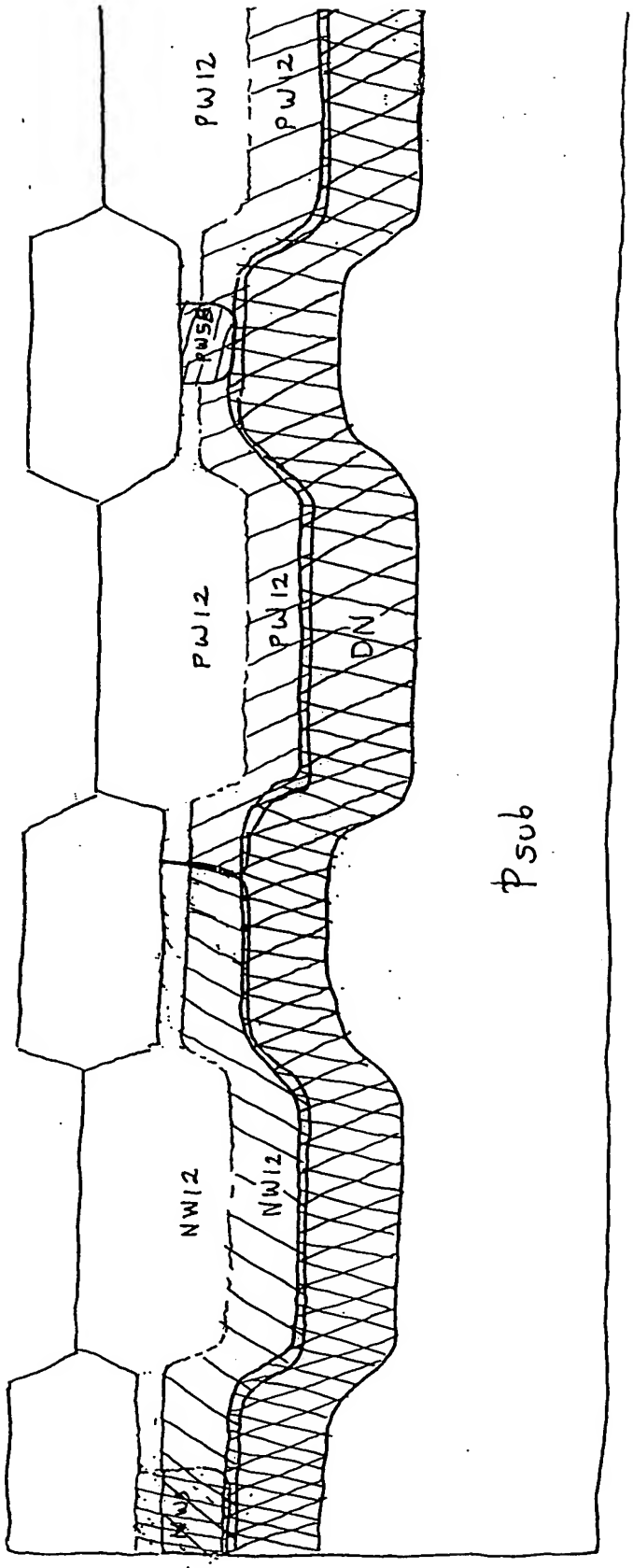
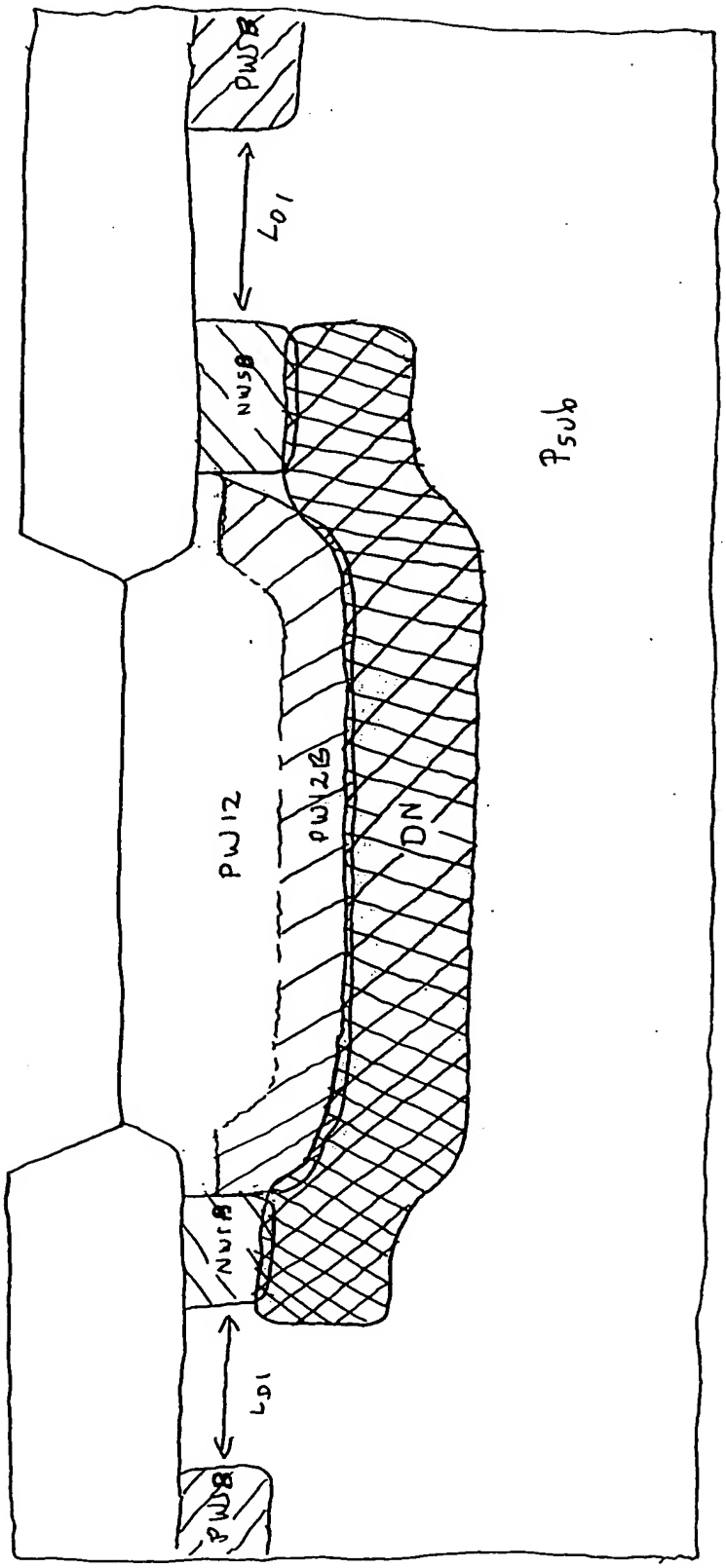


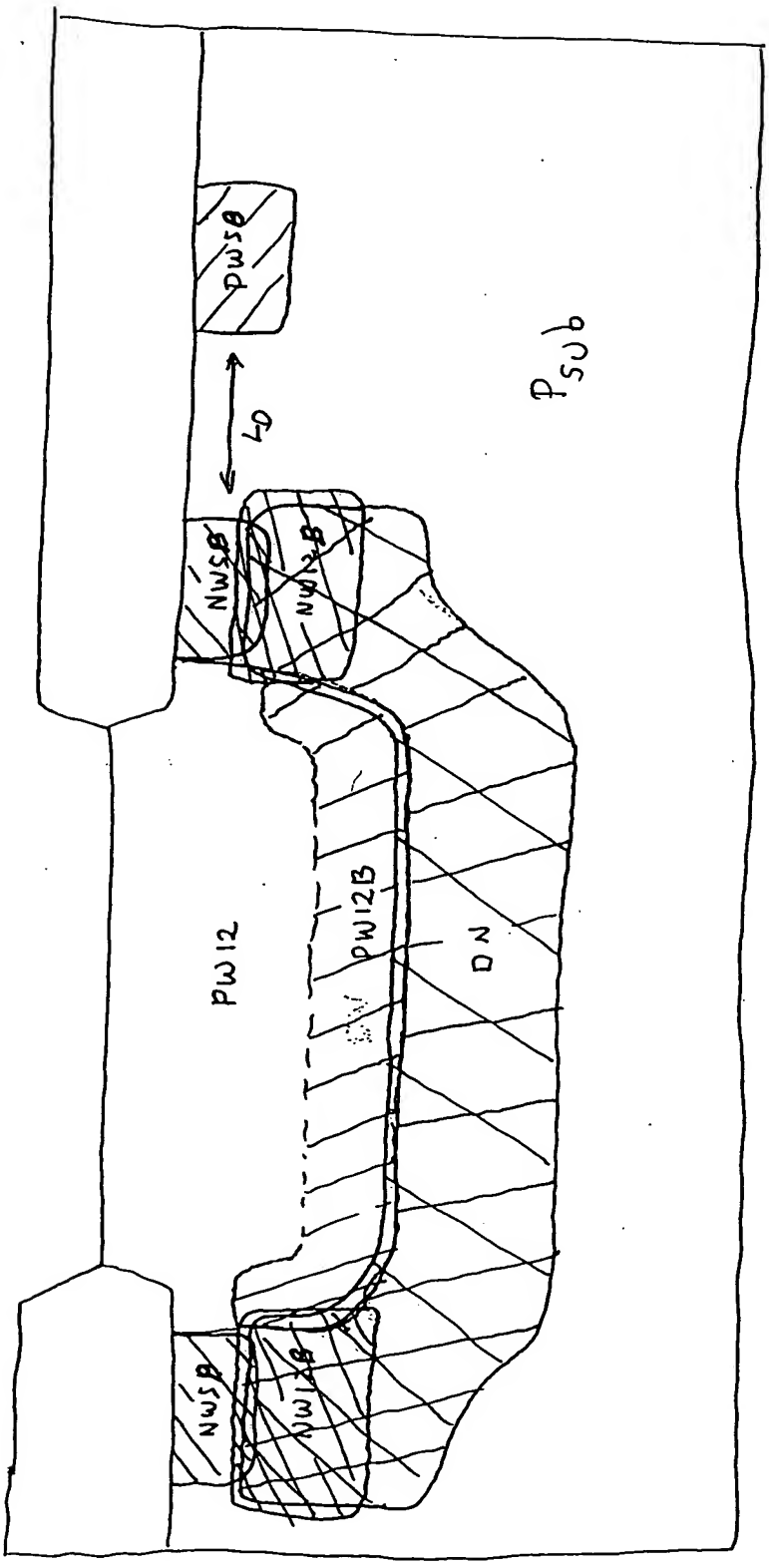
Fig. 15A





Fig, 15B

Fig. 15C



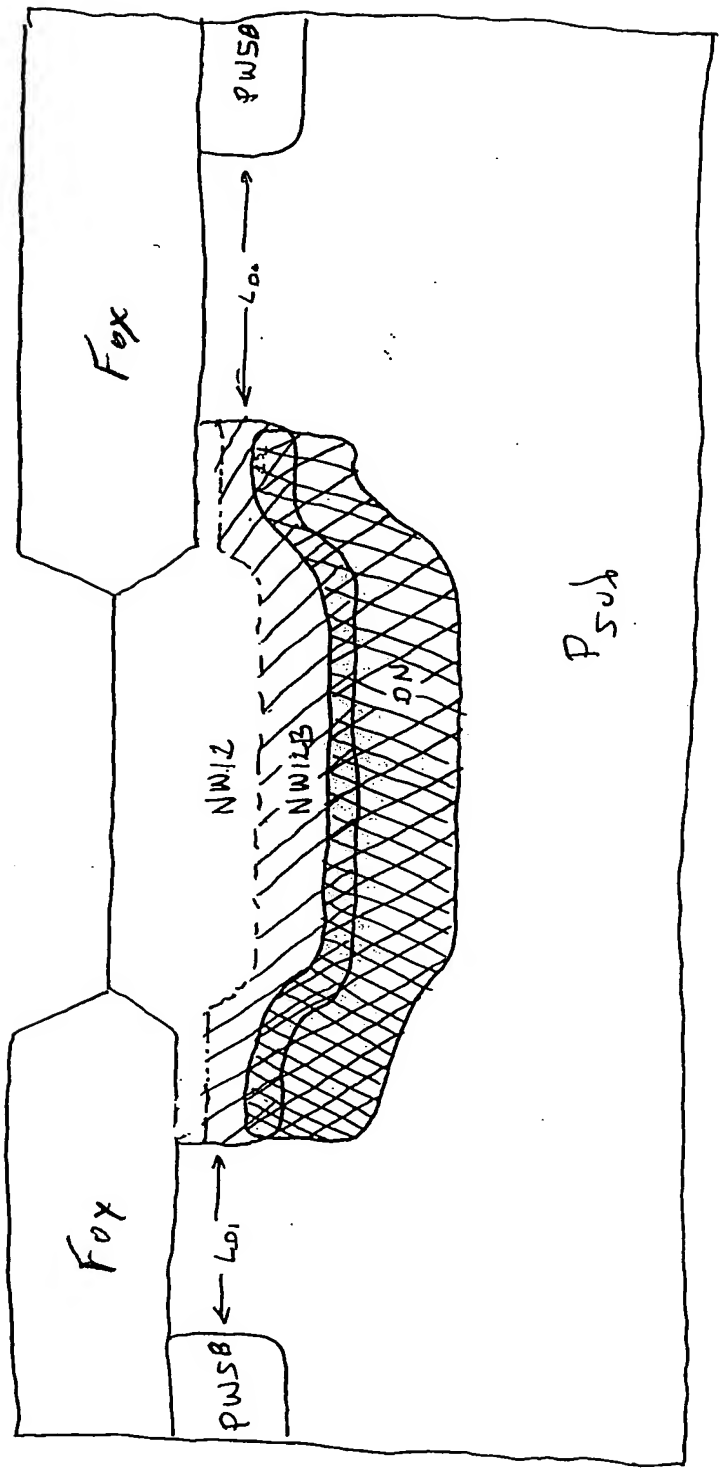


Fig. 15D

Fig. 15F

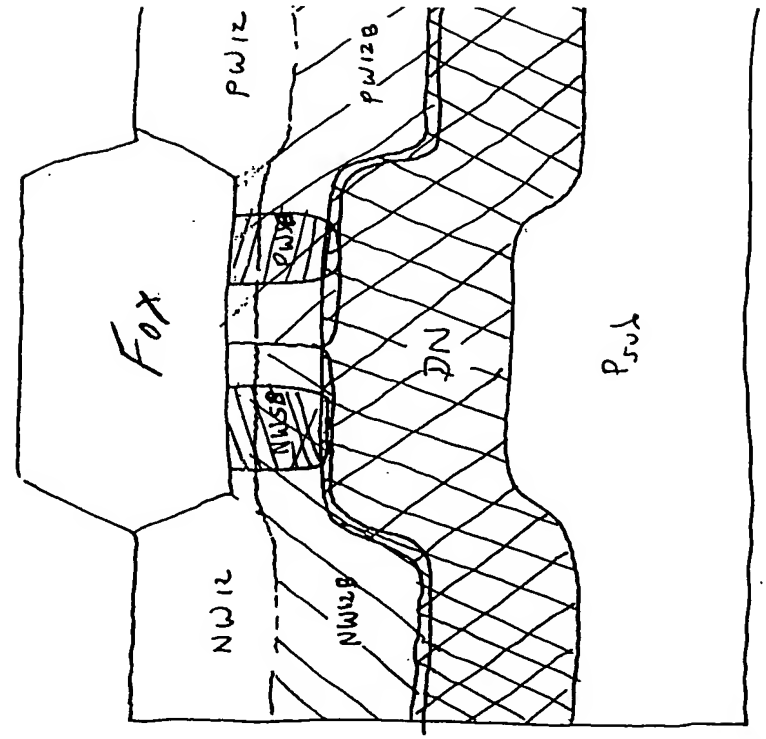
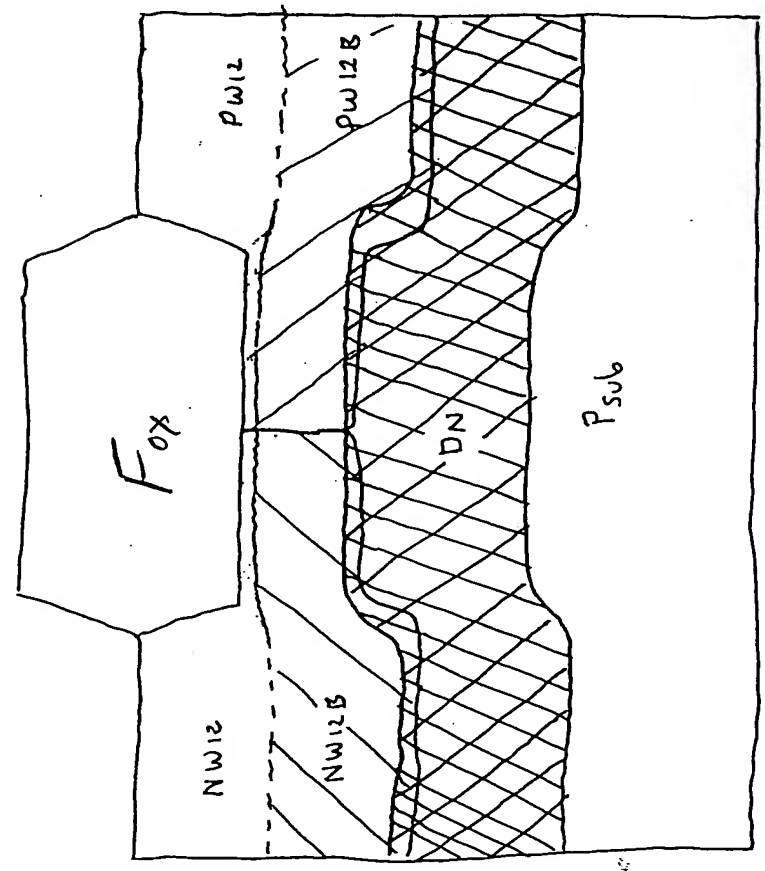


Fig. 15E



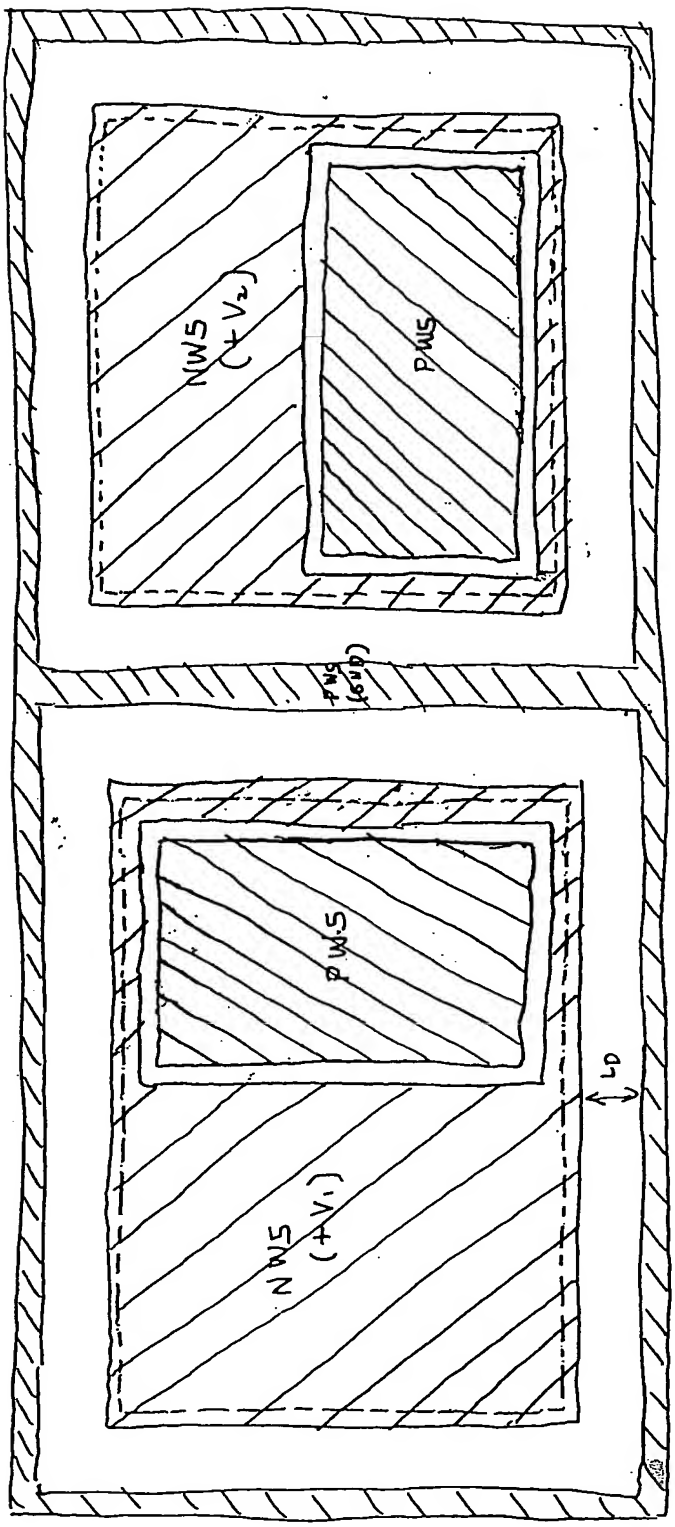
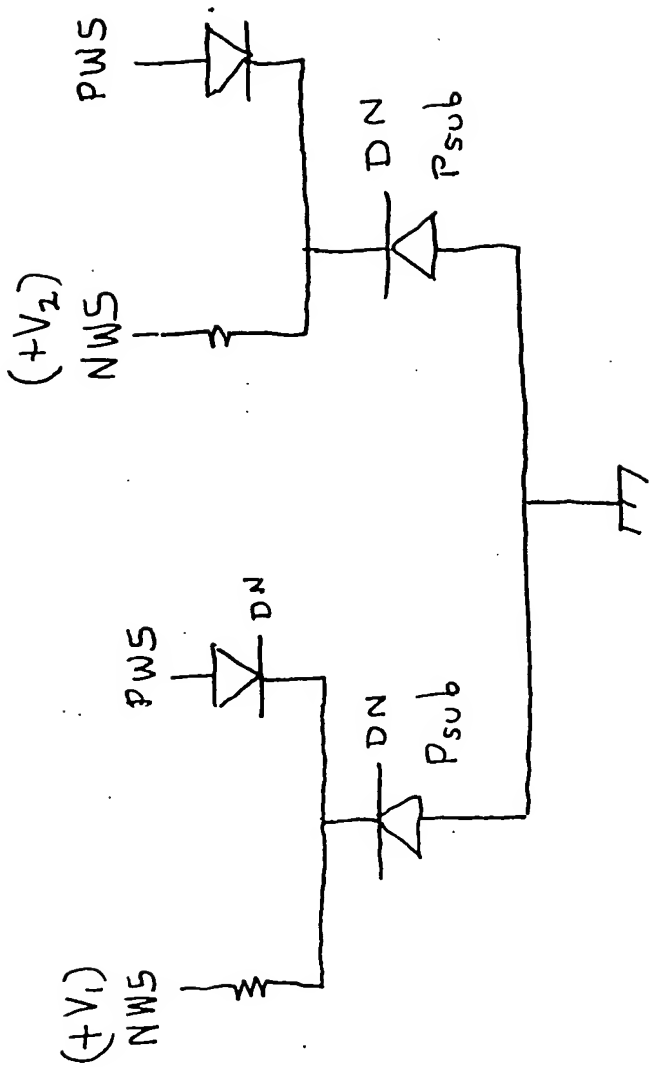


Fig. 16B

Fig. 16C



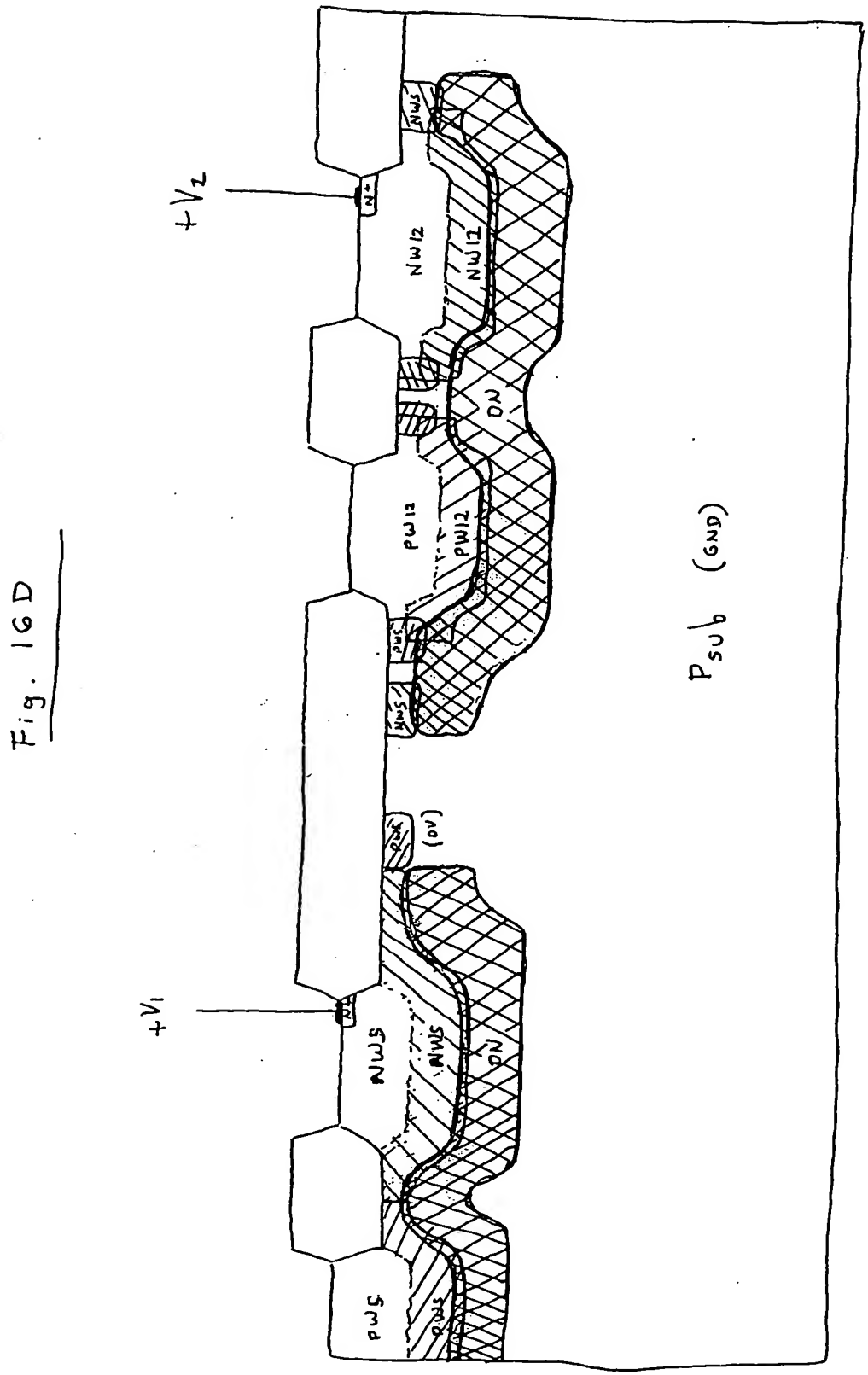
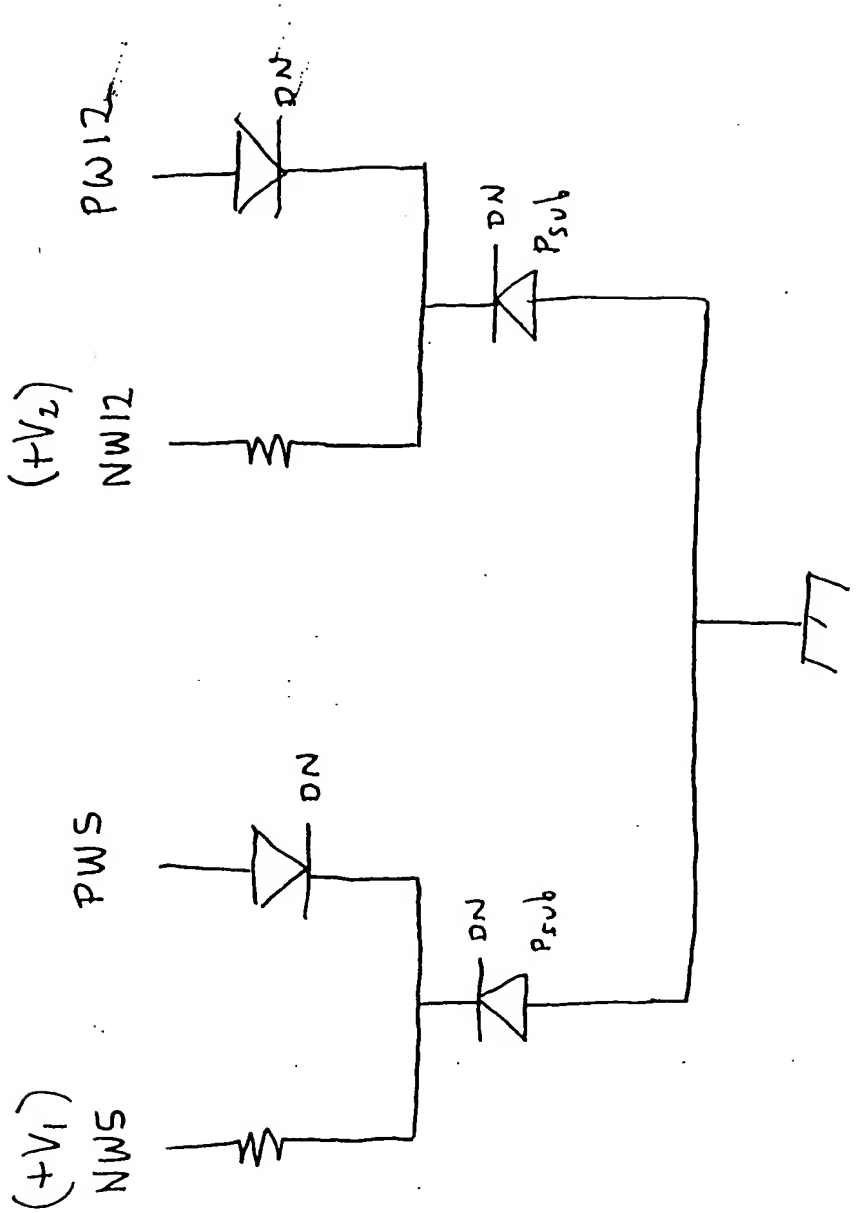

+V2
+V1
NW12
NW12
DN
PW12
PW12
NW35
NW35
DN
PW35
PW35
N+
P+
(0V)
Psub (GND)

Fig. 16D

Fig. 16E



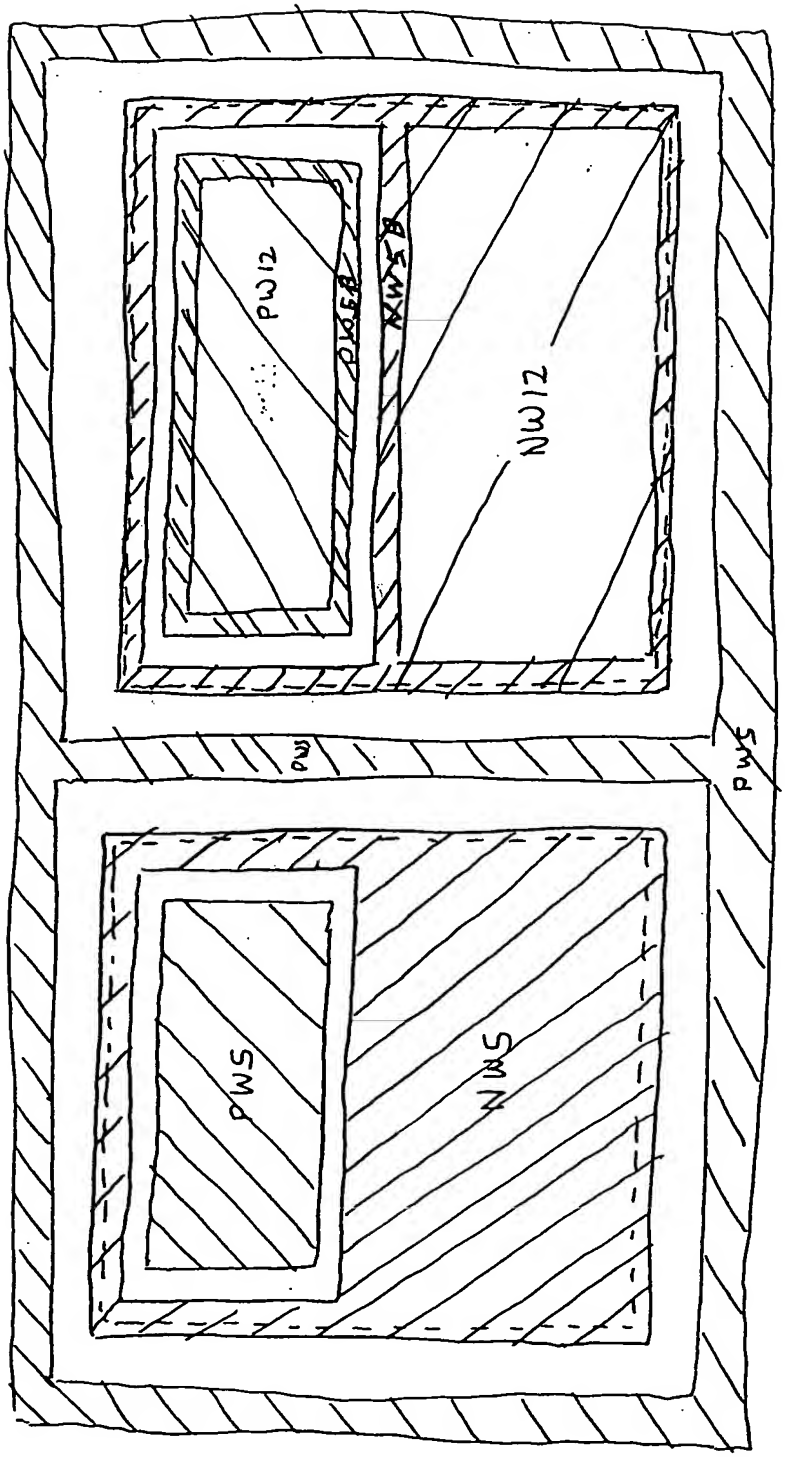


Fig. 16F

Fig. 17A

Prior Art

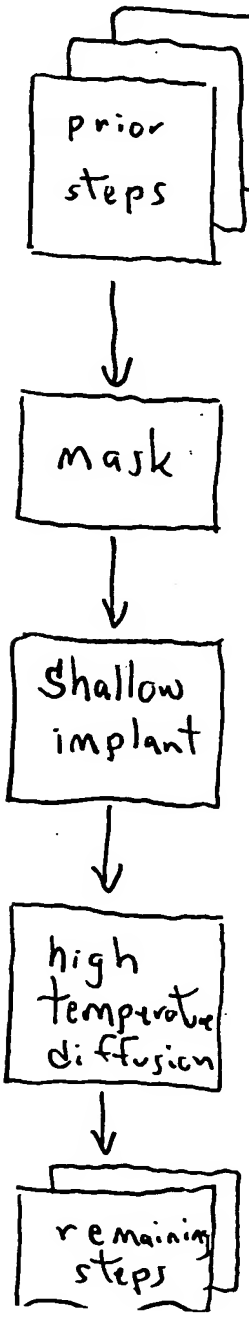


Fig. 17B

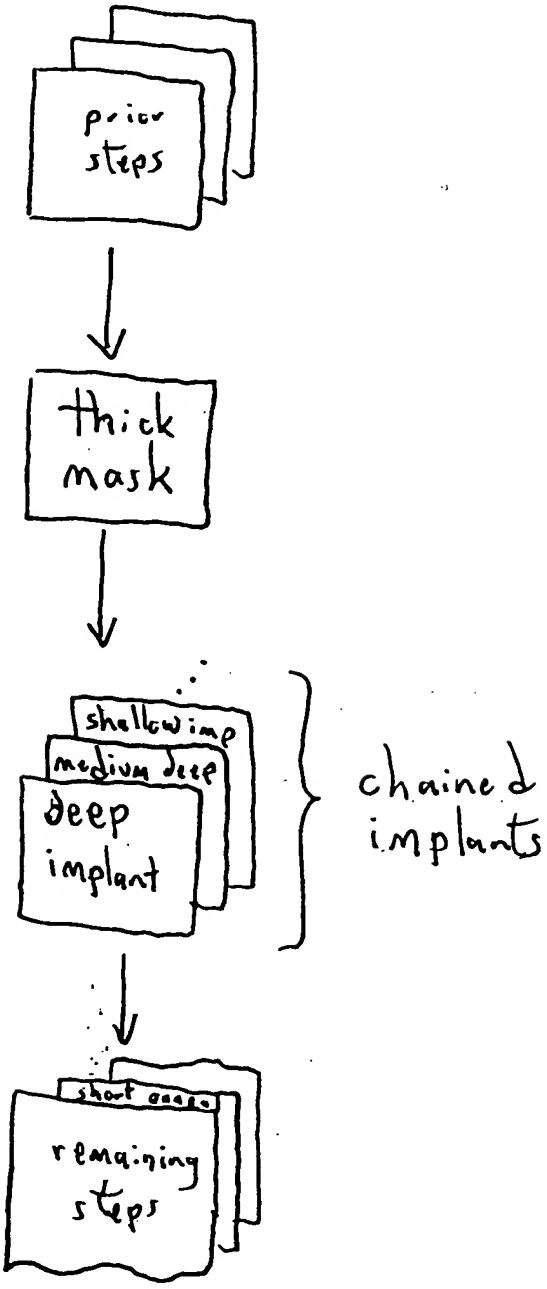


Fig. 17D

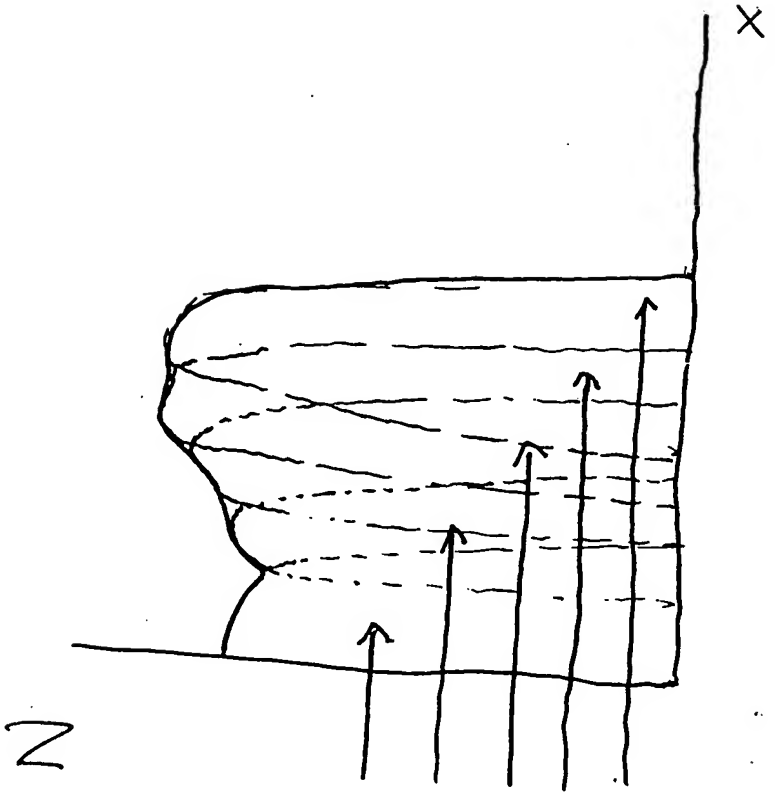


Fig. 17C

Prior Art

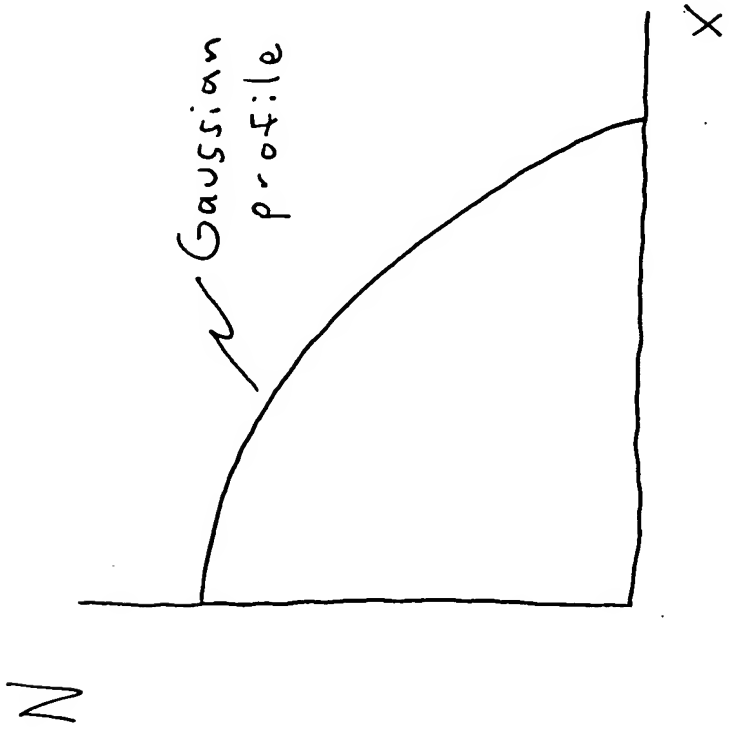


Fig. 17F

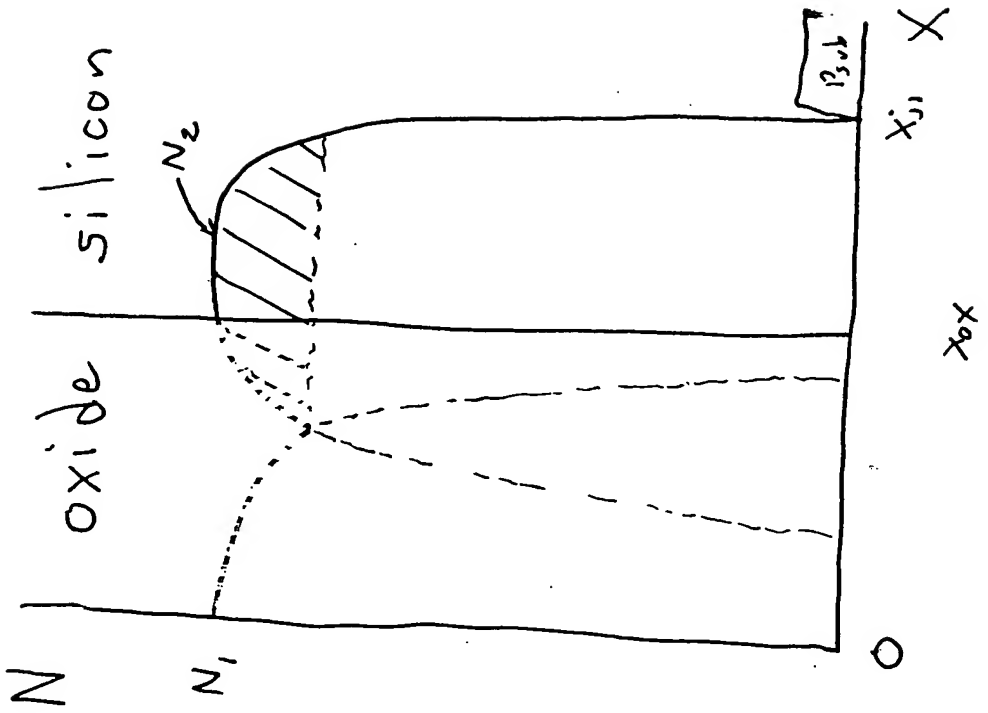


Fig. 17E

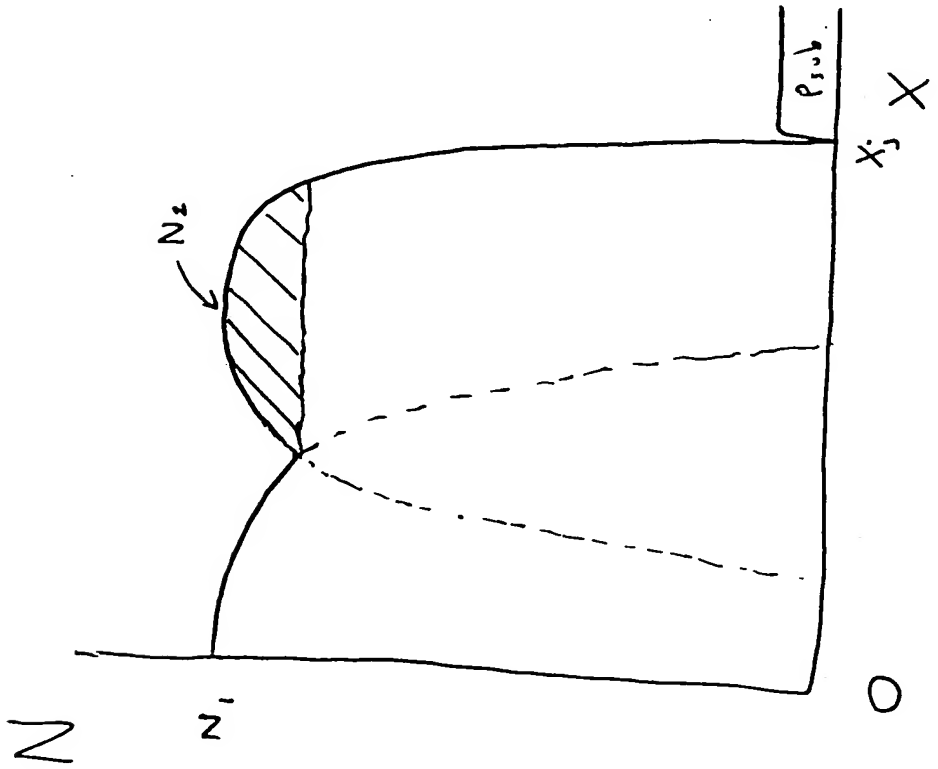


Fig. 17H

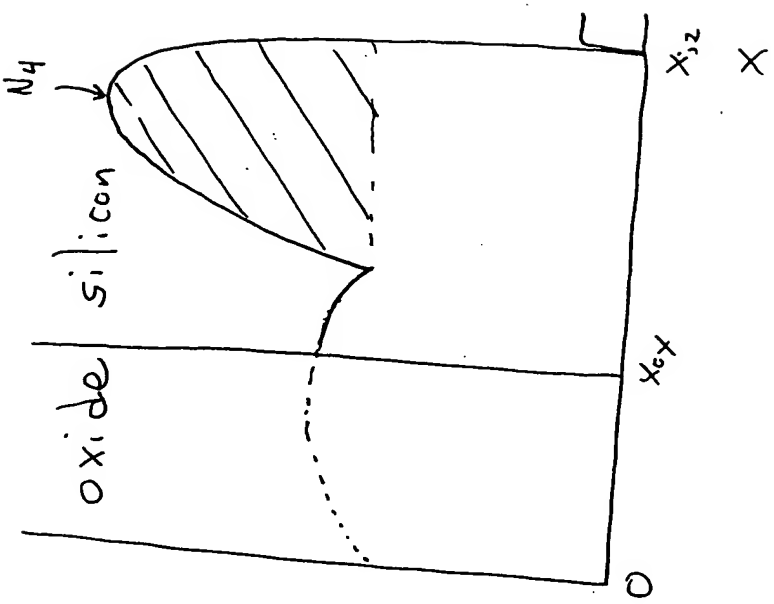


Fig. 17G

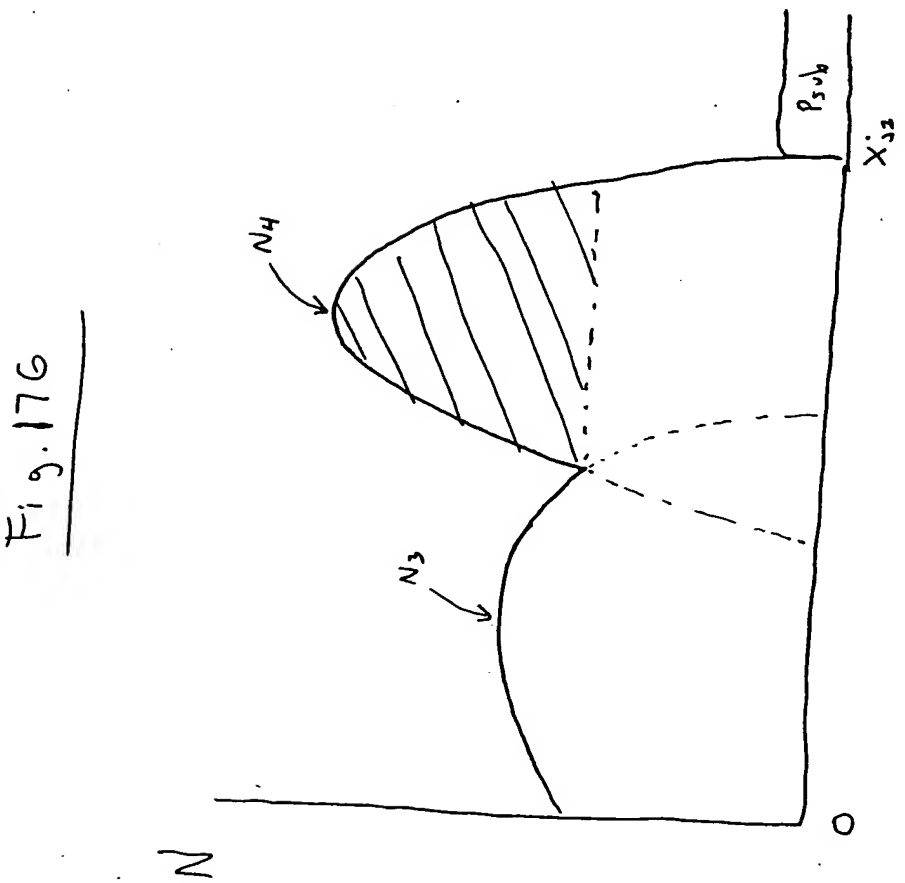


Fig. 17J

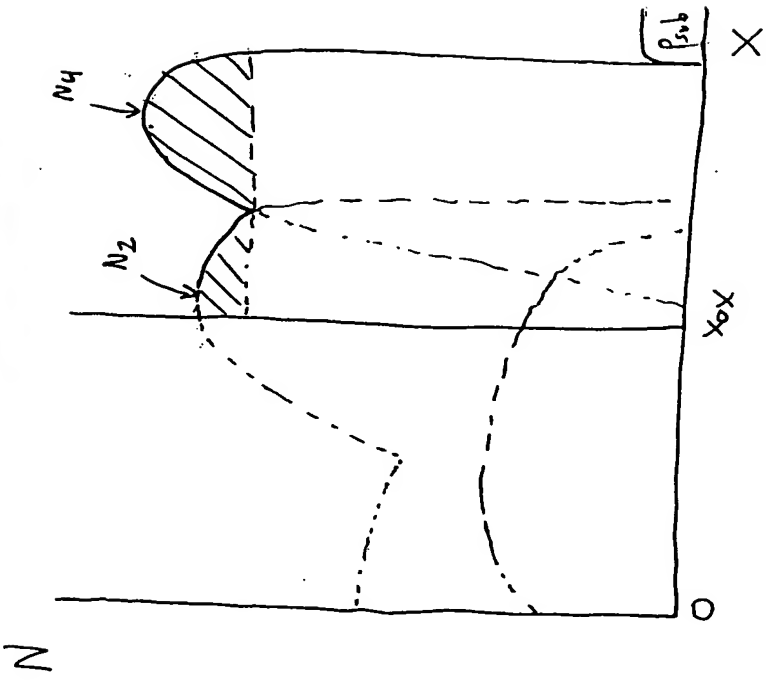
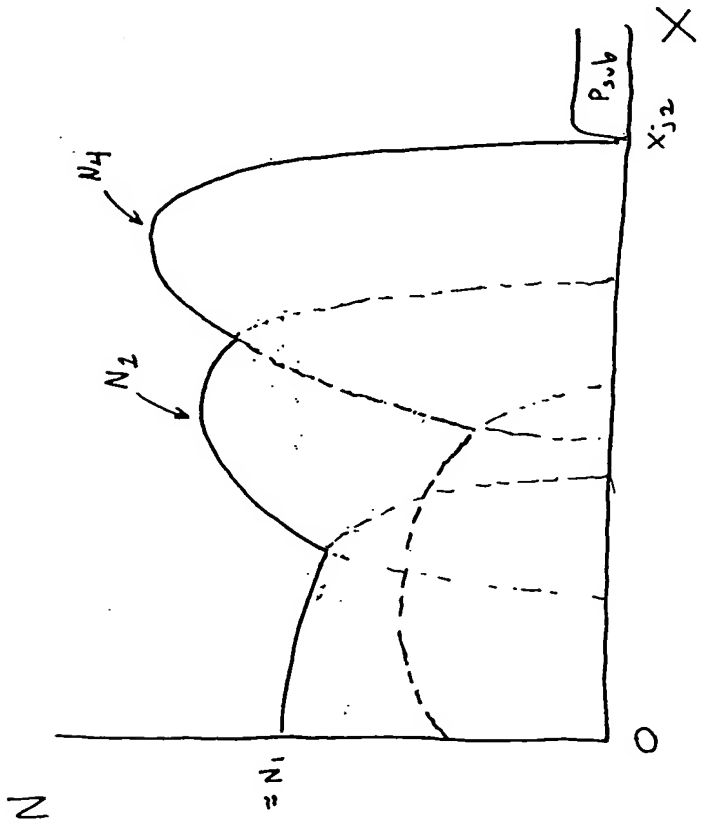


Fig. 17I



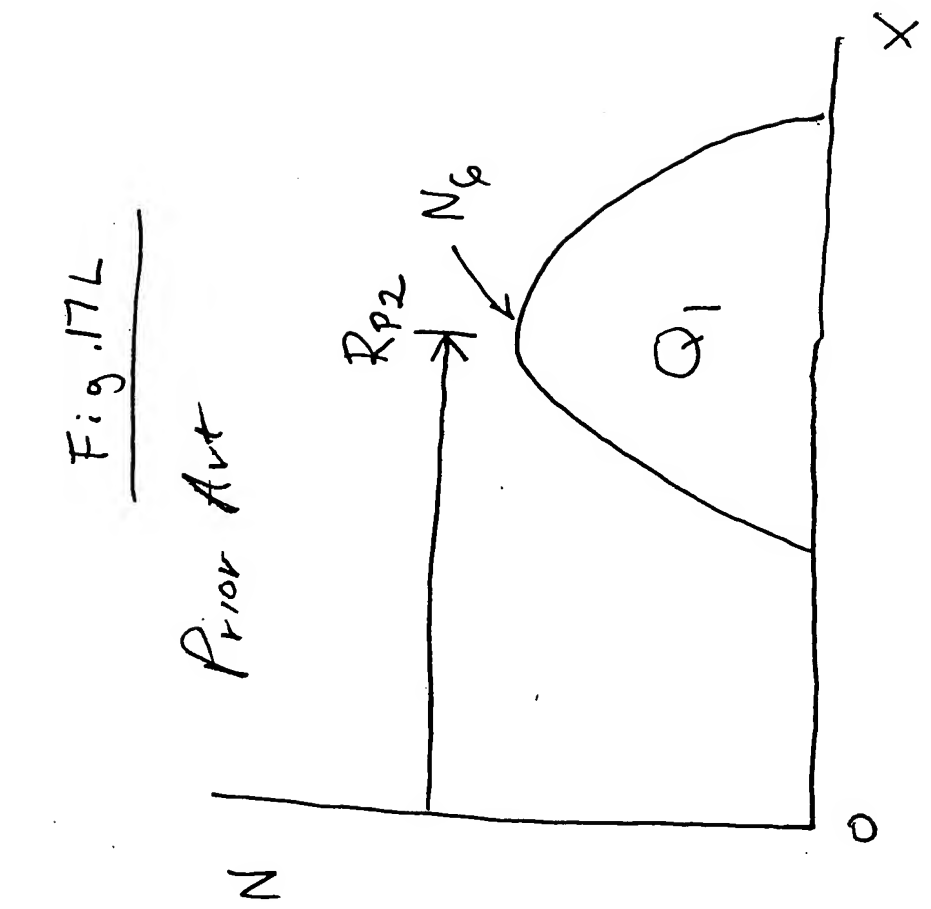


Fig. 17L
Prior Art

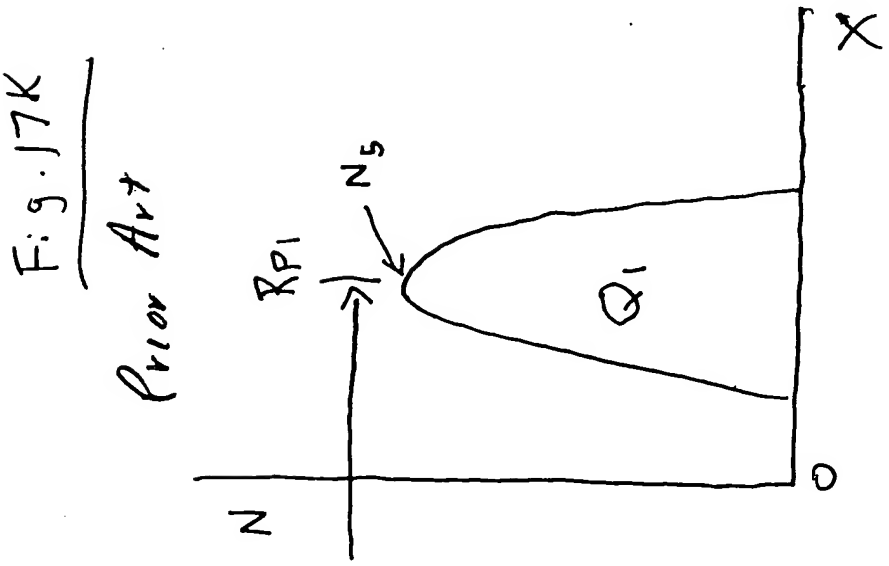


Fig. 17K
Prior Art

Fig. 17N

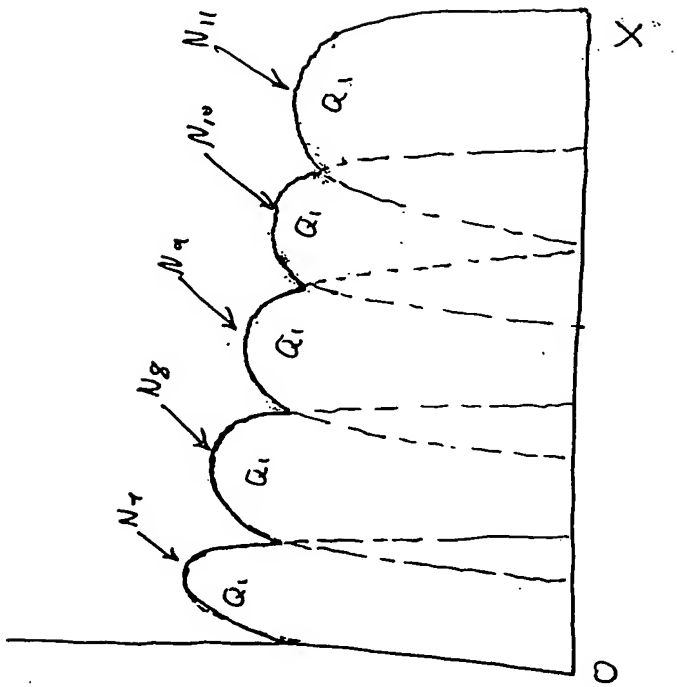


Fig. 17M

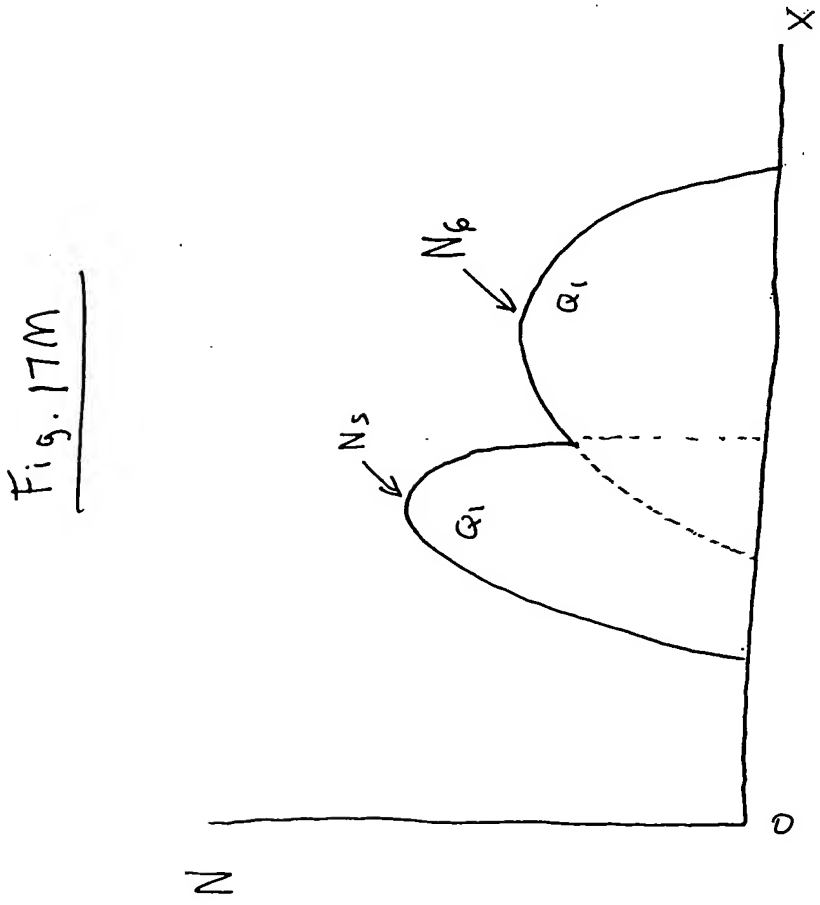


Fig. 17Q

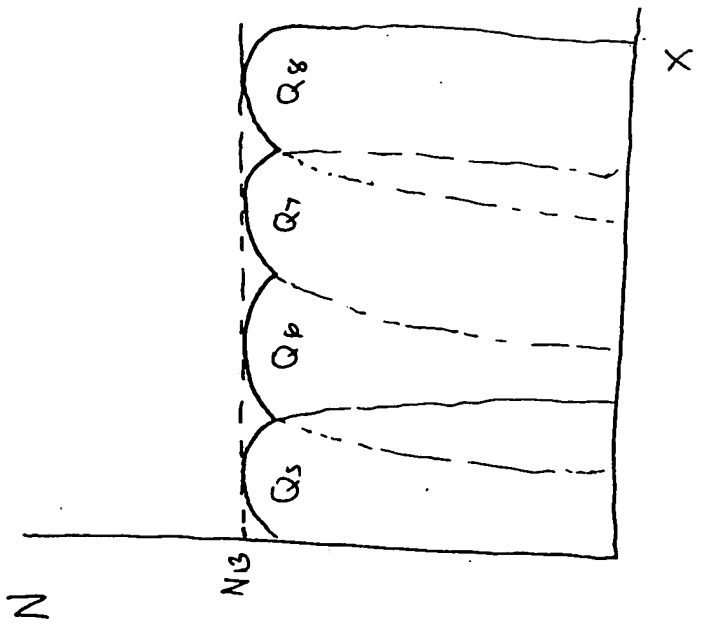


Fig. 17P

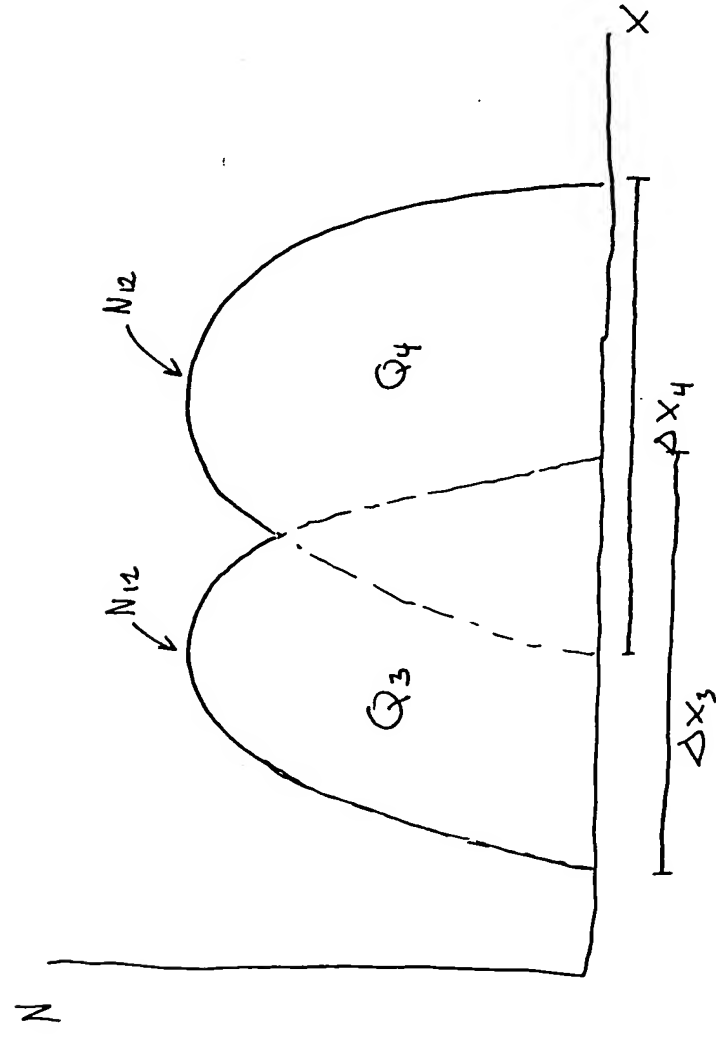


Fig. 17S

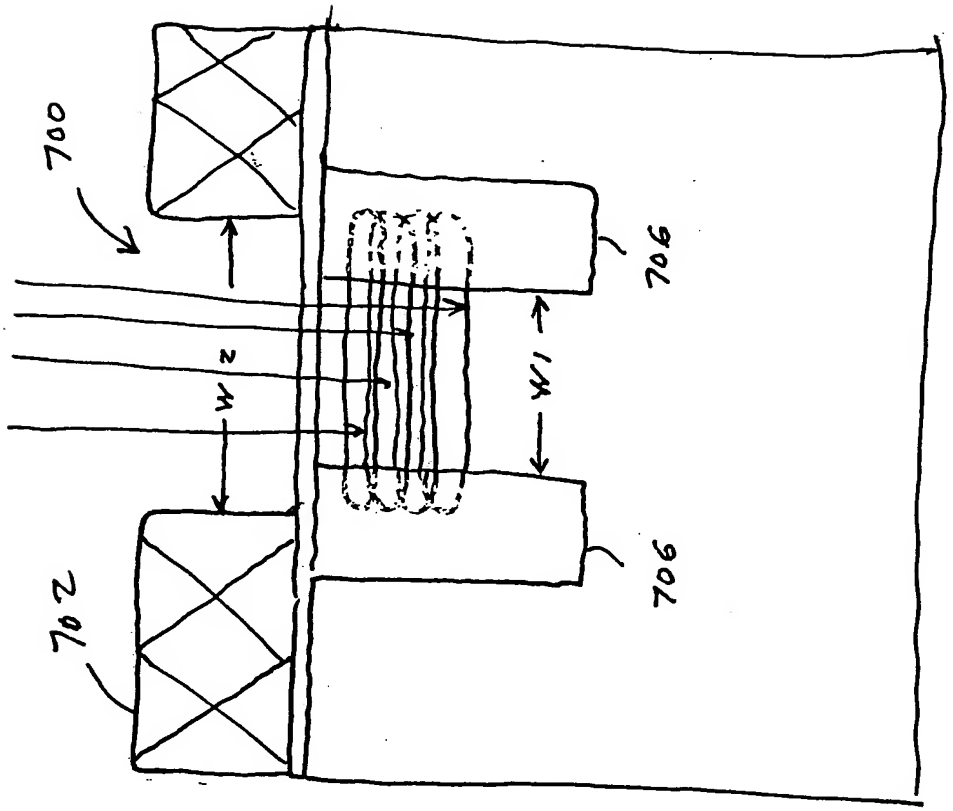


Fig. 17R

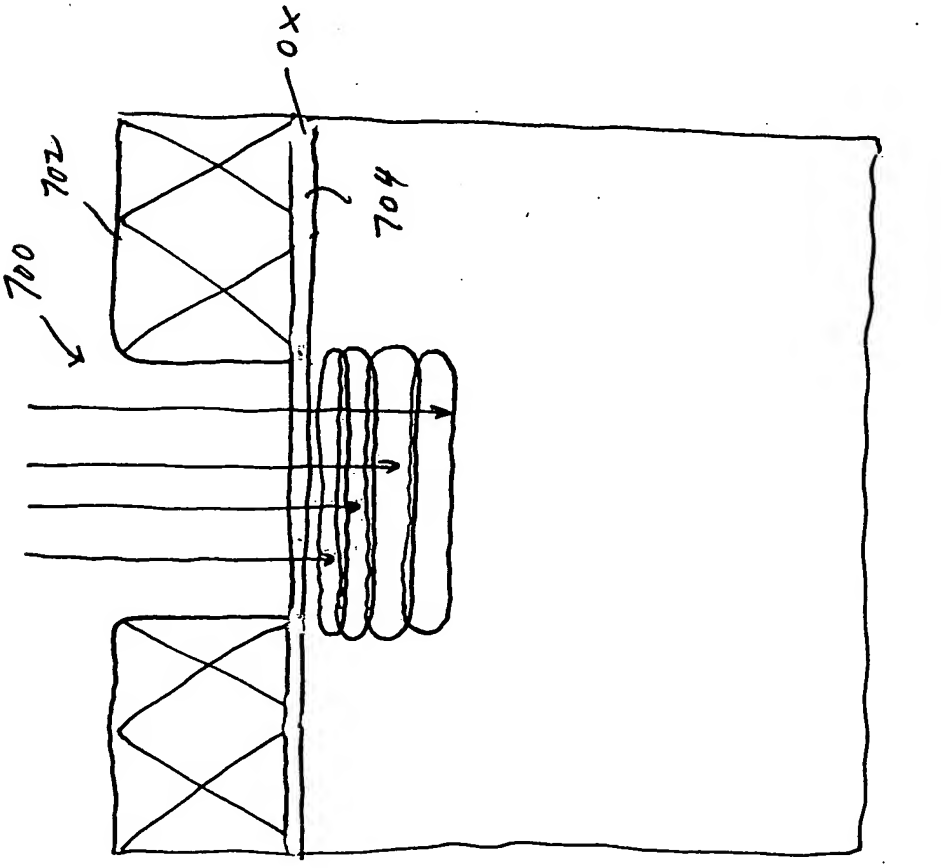


Fig. 17U

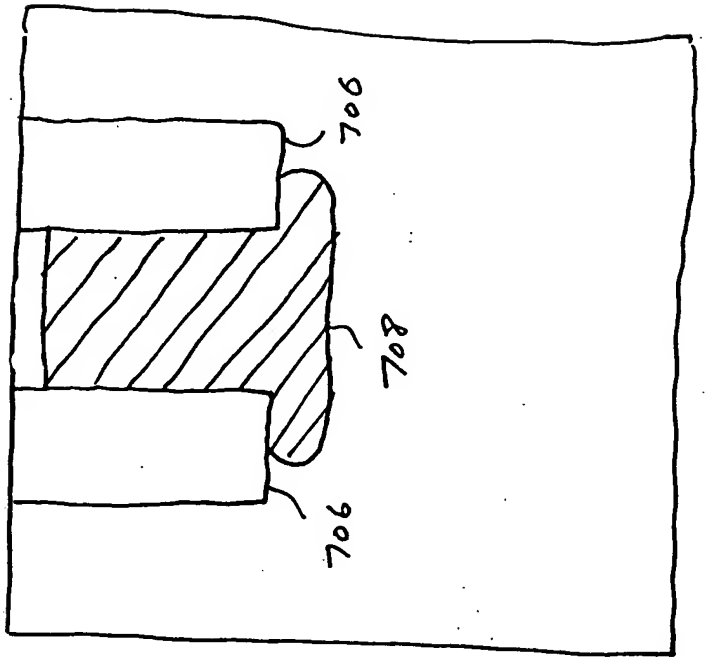
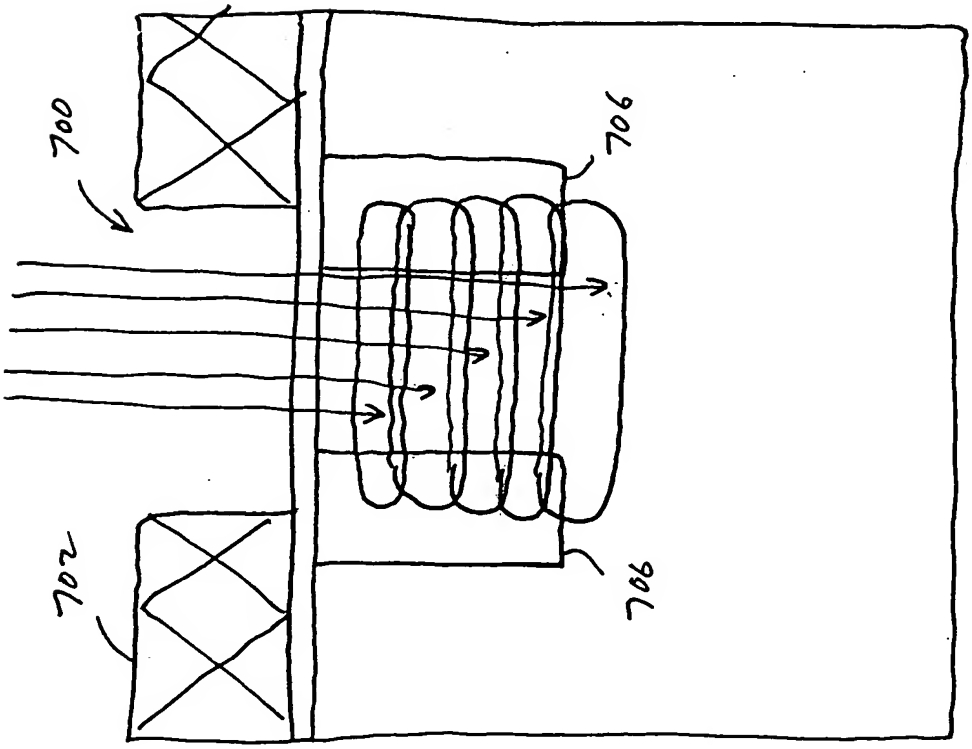


Fig. 17T



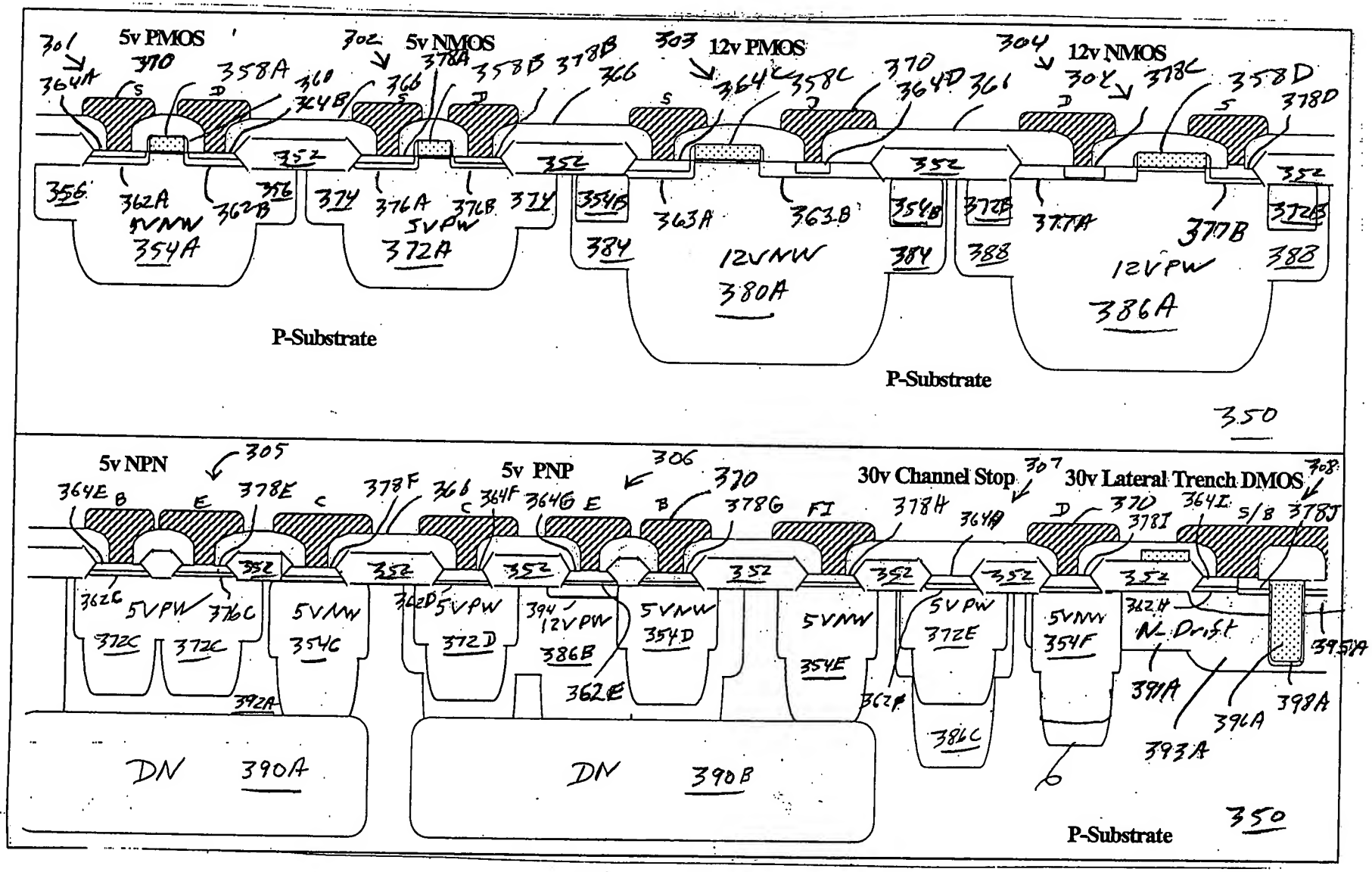

5v PMOS
5v NMOS
12v PMOS
12v NMOS
P-Substrate
5v NPN
5v PNP
30v Channel Stop
30v Lateral Trench DMOS
5VNW
5VPW
12VNW
12VPW
N_Drift
DN
P-Substrate
350

Fig. 18A

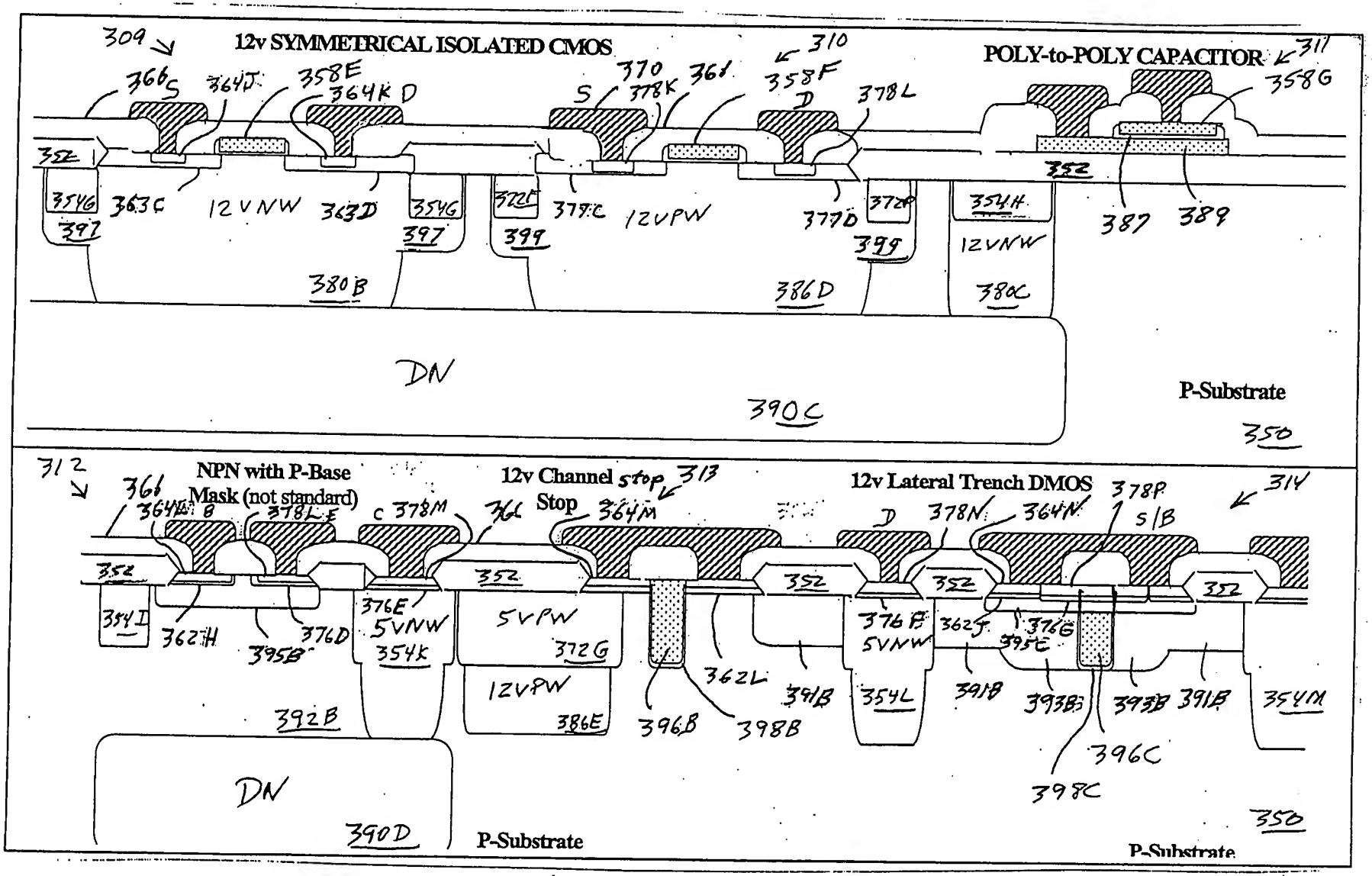

12v SYMMETRICAL ISOLATED CMOS
POLY-to-POLY CAPACITOR
NPN with P-Base Mask (not standard)
12v Channel Stop
12v Lateral Trench DMOS
12VNW
12VPW
5VNW
5VPW
DN
P-Substrate

Fig. 18B

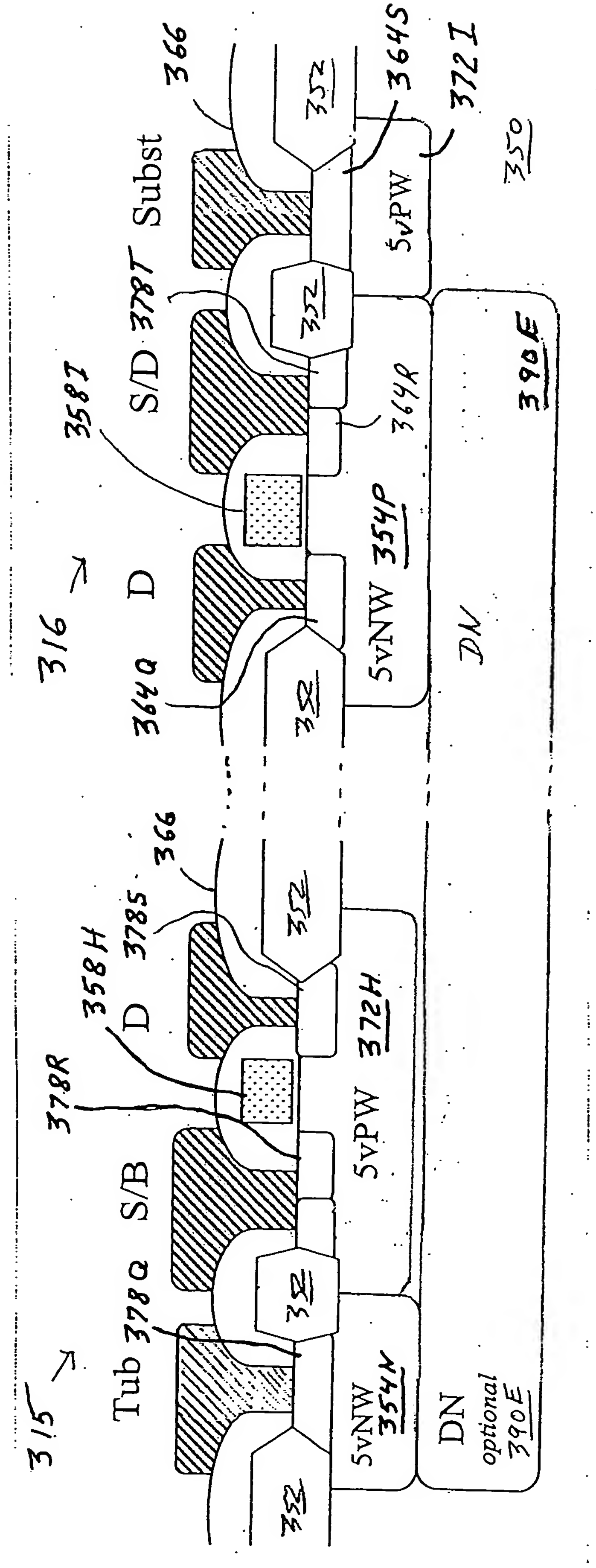

315
316
Tub
S/B
D
D
S/D
Subst
378Q
378R
358H
378S
366
364Q
358I
378T
364S
366
372I
350
364R
352
5vNW
354N
5vPW
372H
5vNW
354P
5vPW
DN
optional
390E
DN
390E

Fig. 18C

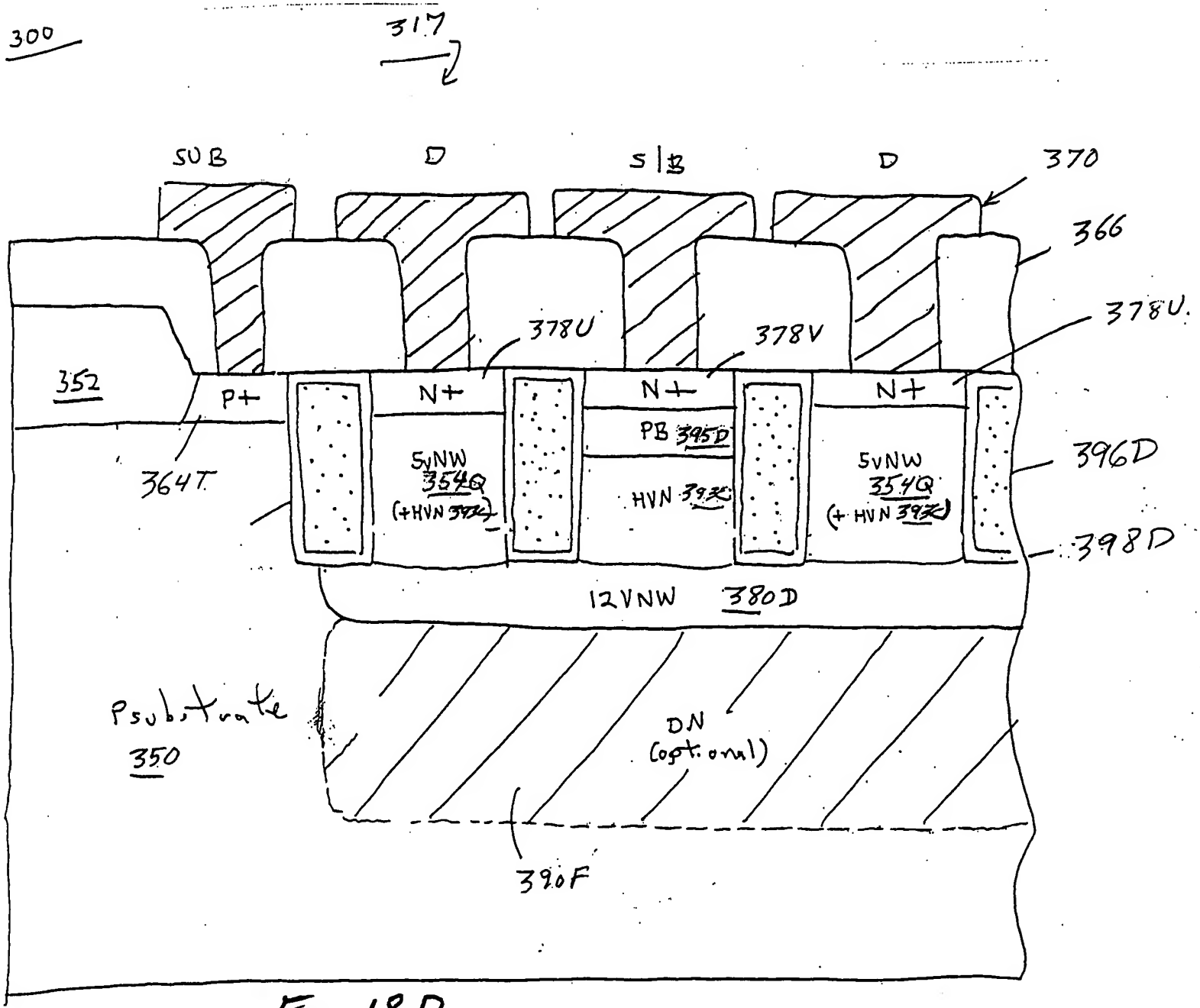

300
317
SUB
D
S/B
D
370
366
378U
378V
378U
352
P+
N+
N+
N+
364T
PB 395D
5VNW 354Q
(+HVN 392)
HVN 392
5VNW 354Q
(+HVN 392)
396D
398D
12VNW 380D
Psubstrate 350
DN (optional)
390F

Fig. 18D

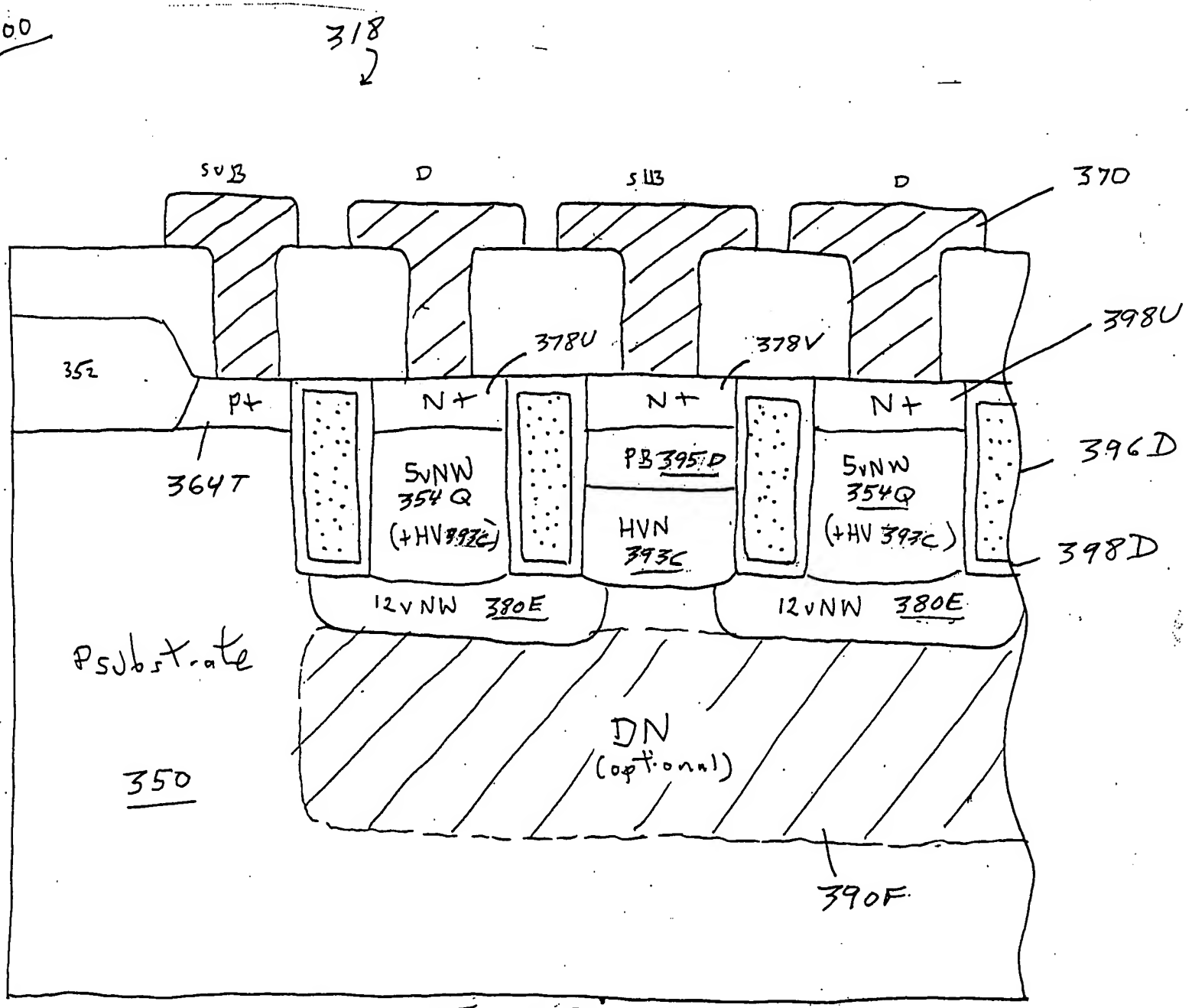

300
318
SUB
D
SUB
D
370
398U
378U
378V
352
P+
N+
N+
N+
364T
5VNW
354Q
(+HV 397C)
PB 395D
HVN
397C
5VNW
354Q
(+HV 397C)
396D
398D
12VNW 380E
12VNW 380E
PSUBSTRATE
DN
(optional)
350
390F

Fig. 18E

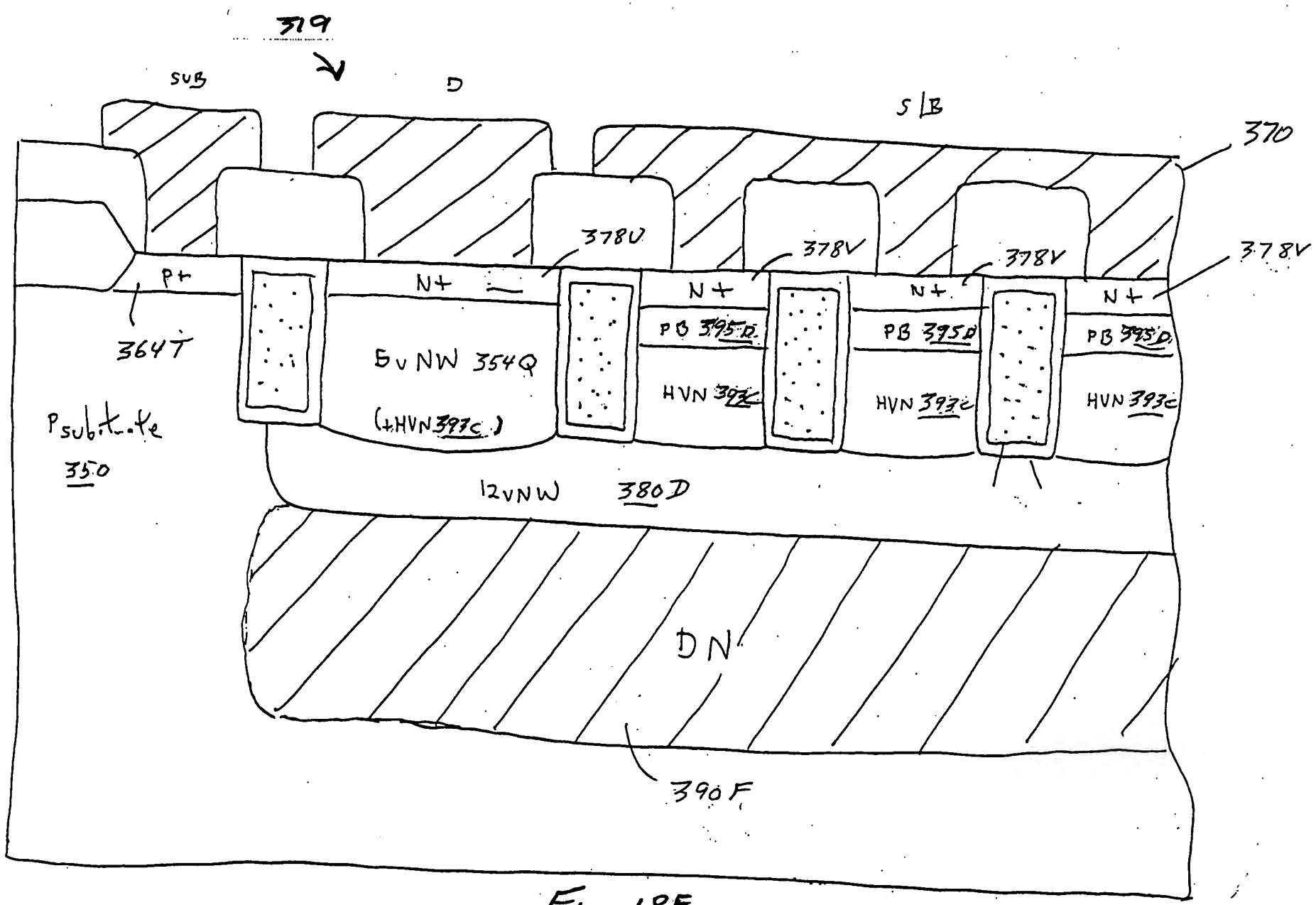

319
SUB
D
S
B
370
378V
378V
378V
378V
P+
N+
N+
N+
N+
364T
PB 395D
PB 395D
PB 395D
5vNW 354Q
(+HVN 397C)
HVN 397C
HVN 397C
HVN 397C
Psubstrate
350
12vNW 380D
DN
390F

Fig. 18F

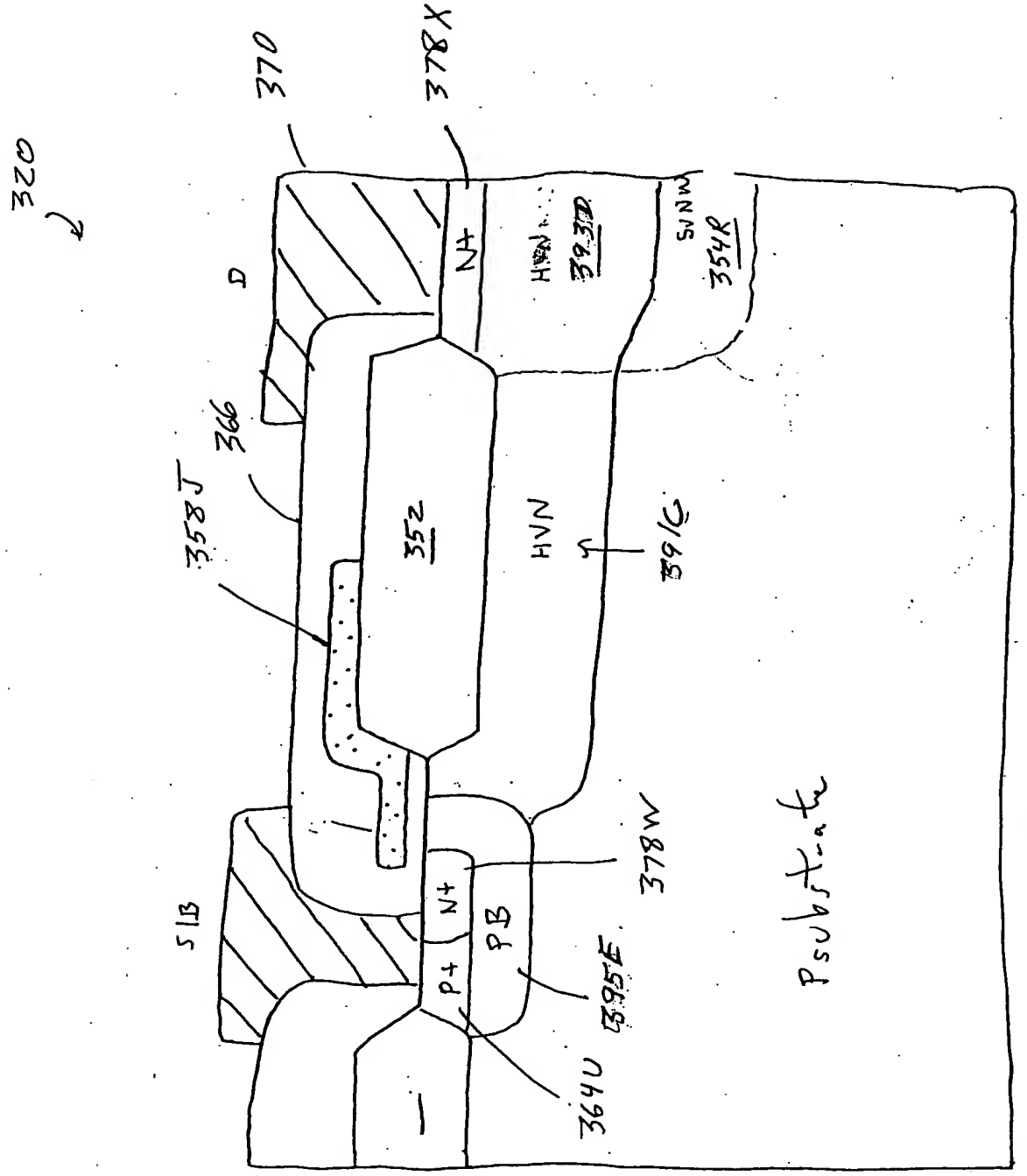
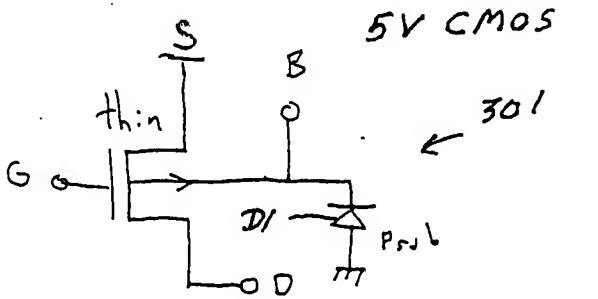

320
370
378X
D
N+
HVN
354R
366
358J
352
HVN
391G
SUB
P+
N+
PB
378W
364U
395E
Substrate

Fig 18G



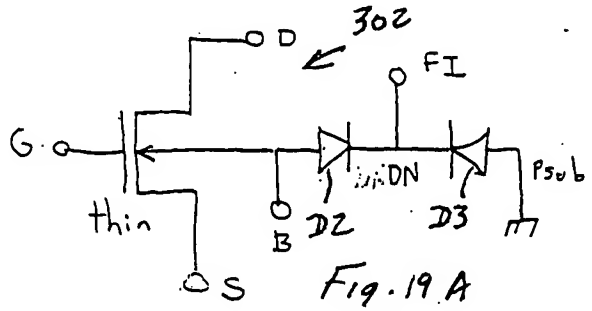
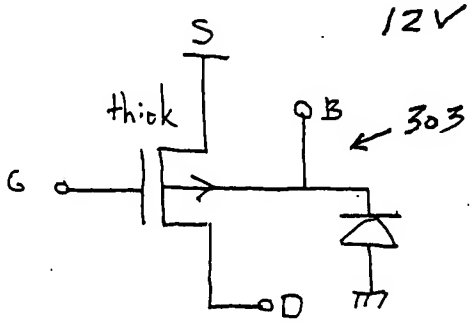


Fig. 19A



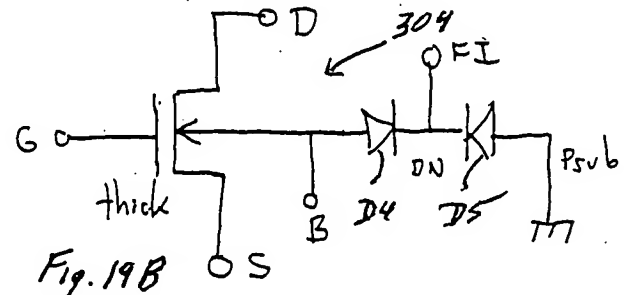


Fig. 19B

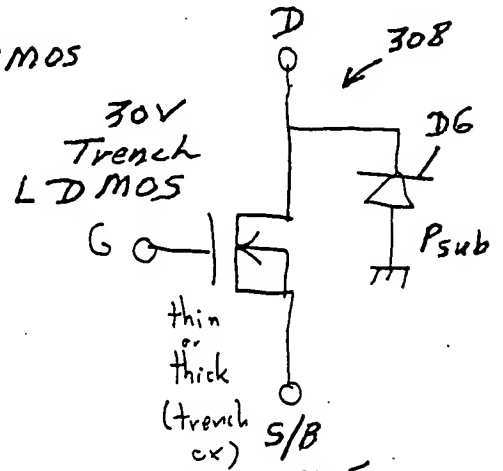


Fig. 19E

5V NPN

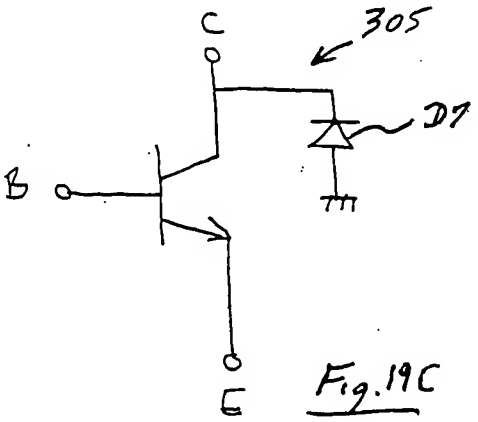


Fig. 19C

5V PNP

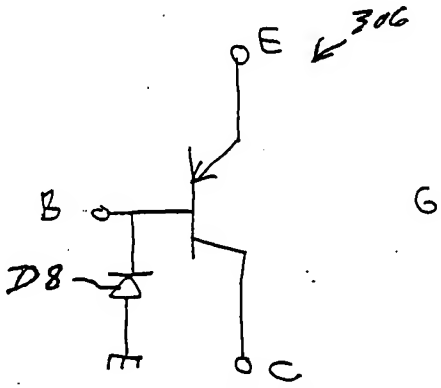


Fig. 19D

30V LDMOS

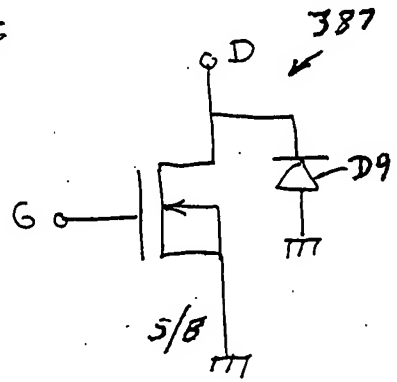


Fig. 19H

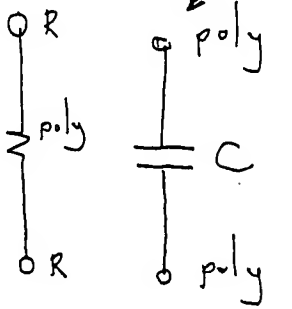
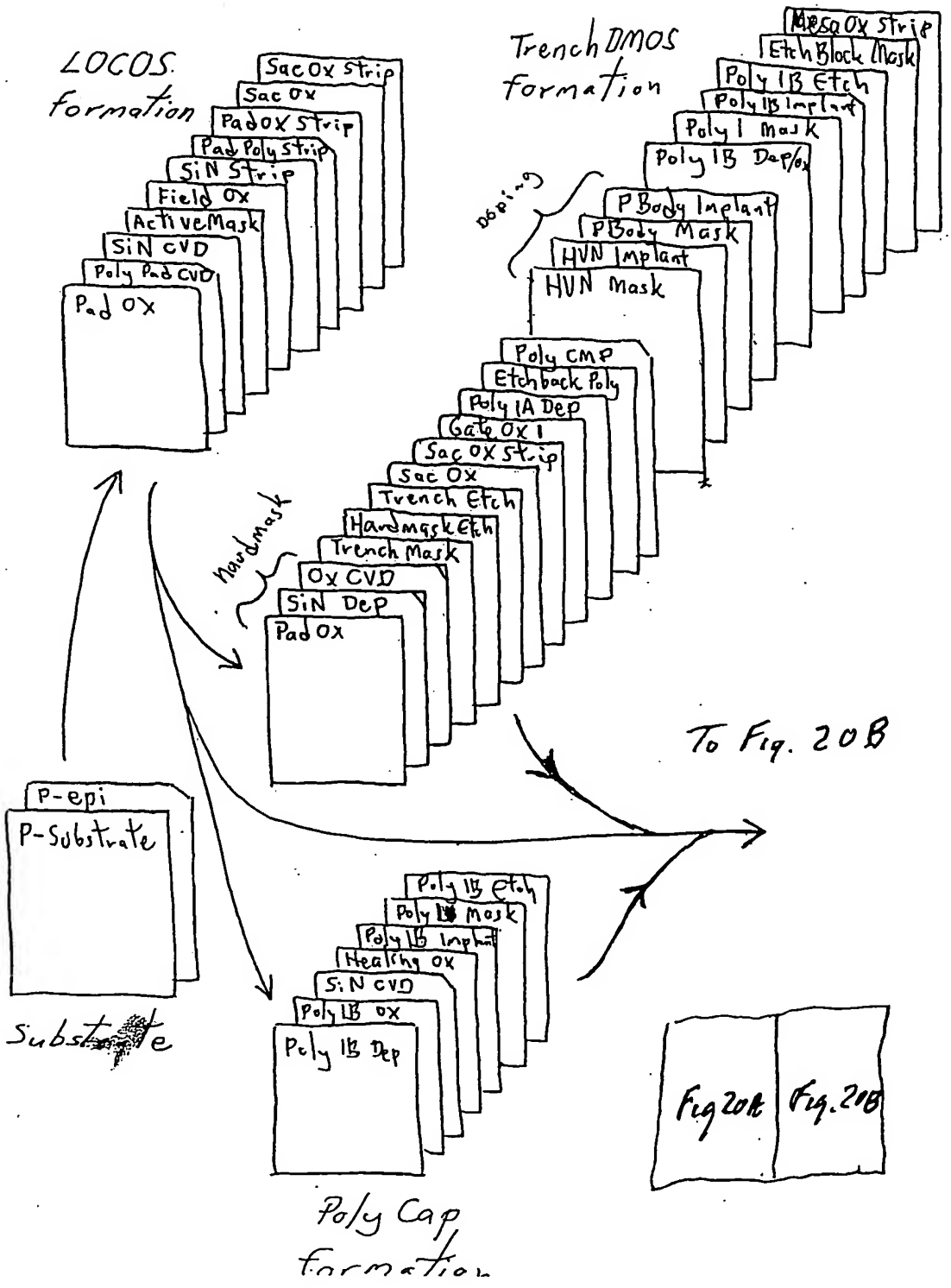


Fig. 19G

Fig. 19F


LOCOS formation
Sac Ox Strip
Sac Ox
Pad Ox Strip
Pad Poly Strip
SiN Strip
Field Ox
Active Mask
SiN CVD
Poly Pad CVD
Pad Ox
Trench DMOS formation
Mesa Ox Strip
Etch Block Mask
Poly 1B Etch
Poly 1B Implant
Poly 1 Mask
Poly 1B Dep/Ox
Doping
P Body Implant
P Body Mask
HVN Implant
HVN Mask
Poly CMP
Etchback Poly
Poly 1A Dep
Gate Ox 1
Sac Ox Strip
Sac Ox
Trench Etch
Hardmask Etch
Trench Mask
Ox CVD
SiN Dep
Pad Ox
Hardmask
To Fig. 20B
P-epi
P-Substrate
Substrate
Poly 1B Etch
Poly 1B Mask
Poly 1B Implant
Healing Ox
SiN CVD
Poly 1B Ox
Poly 1B Dep
Poly Cap formation
Fig 20A
Fig 20A
Fig. 20B

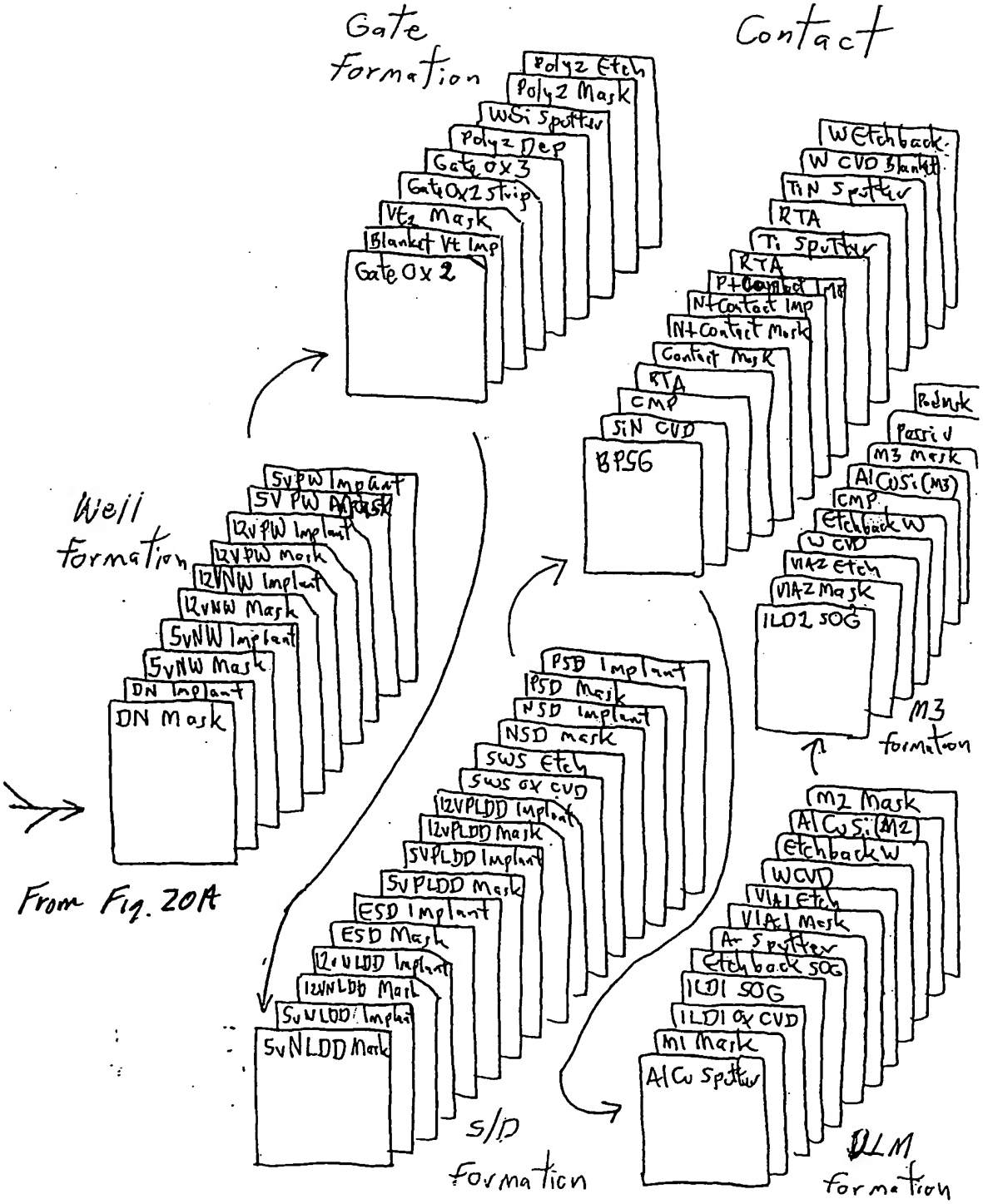

Gate formation
Contact
Well formation
From Fig. 20A
S/D formation
M3 formation
Poly2 Etch
Poly2 Mask
WSi Sputter
Poly2 Dep
Gate Ox3
Gate Ox2 Strip
Vt2 Mask
Blanket Vt Imp
Gate Ox 2
5VPW Implant
5V PW Mask
12VPW Implant
12VPW Mask
12VNW Implant
12VNW Mask
5VNW Implant
5VNW Mask
DN Implant
DN Mask
5VNLDD Implant
5VNLDD Mask
12VNLDD Implant
12VNLDD Mask
5VPLDD Implant
5VPLDD Mask
ESD Implant
ESD Mask
12VPLDD Implant
12VPLDD Mask
SWS Etch
SWS Ox CVD
NSD Implant
NSD mask
PSD Implant
PSD Mask
SiN CVD
BPSG
RTA
CMP
Contact Mask
N+Contact Imp
N+Contact Mask
P+Contact
RTA
Ti Sputter
RTA
TiN Sputter
W CVD Blanket
W Etchback
ILD1 SOG
VIA2 Mask
VIA2 Etch
W CVD
Etchback W
CMP
AlCuSi (M3)
M3 Mask
Passiv
Pad mask
AlCu Sputter
M1 Mask
ILD1 Ox CVD
ILD1 SOG
Etchback SOG
Ar Sputter
VIA1 Mask
VIA1 Etch
W CVD
Etchback W
AlCuSi (M2)
M2 Mask
ILM formation

Fig. 20B

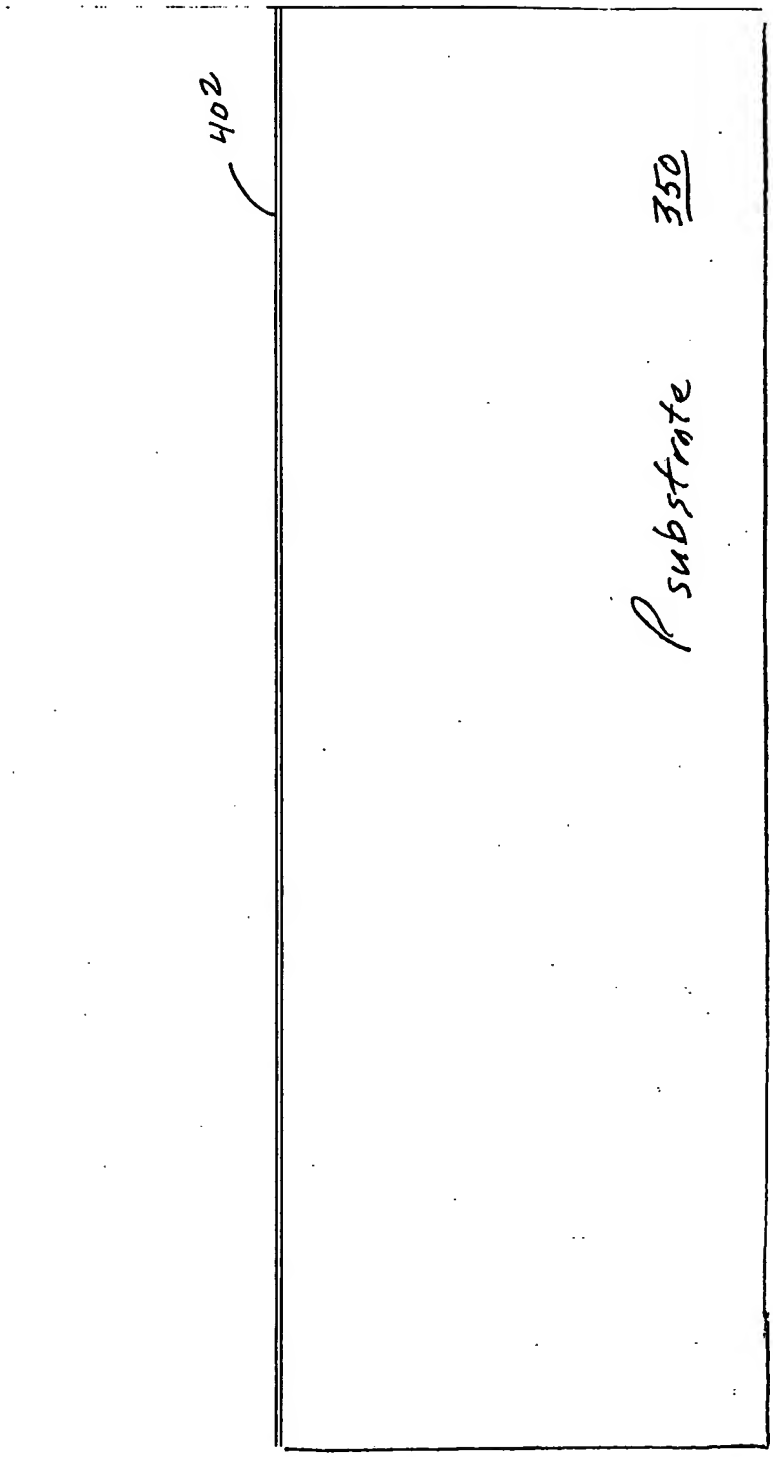
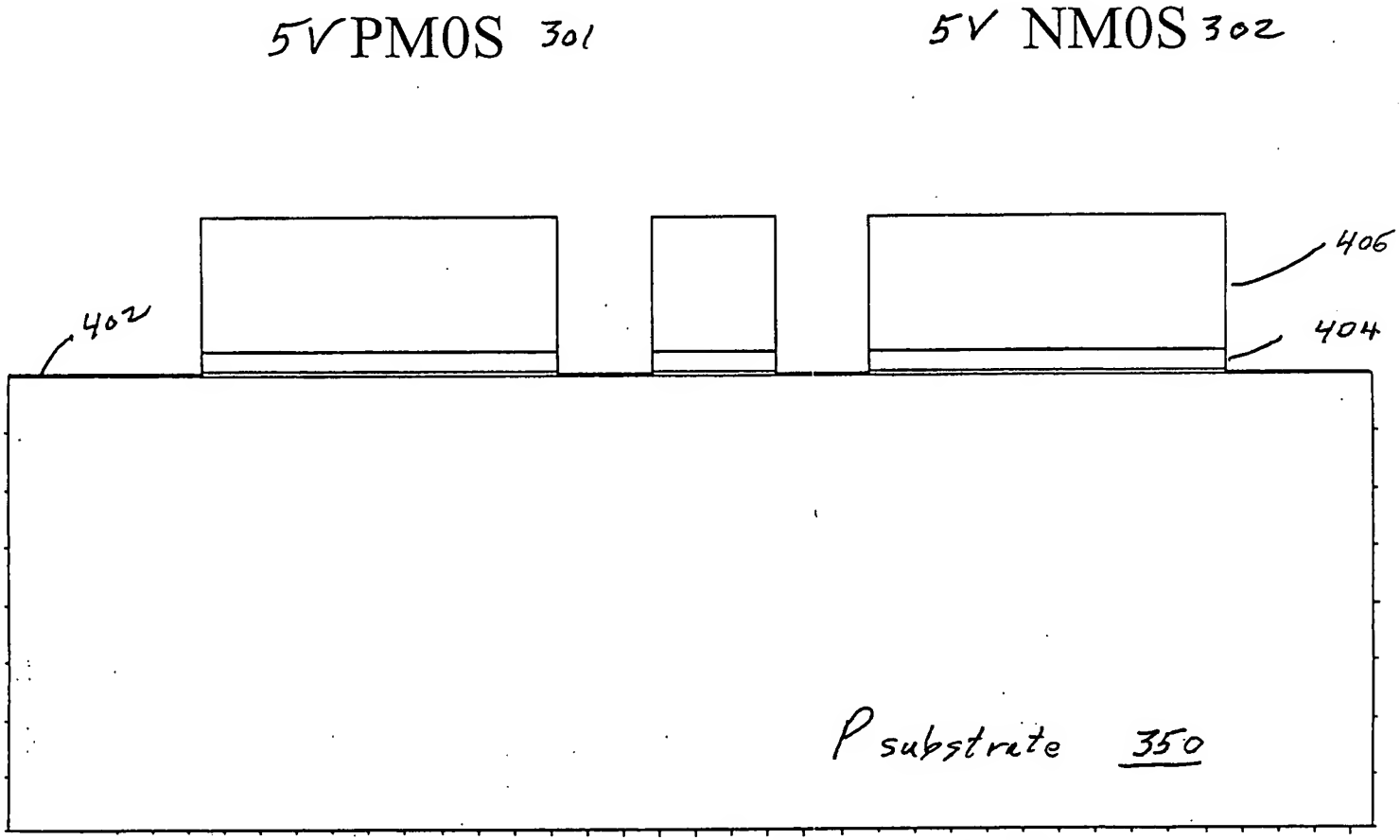


Fig. 21



LOCOS - Nitride Mask and Etch

Fig. 22A

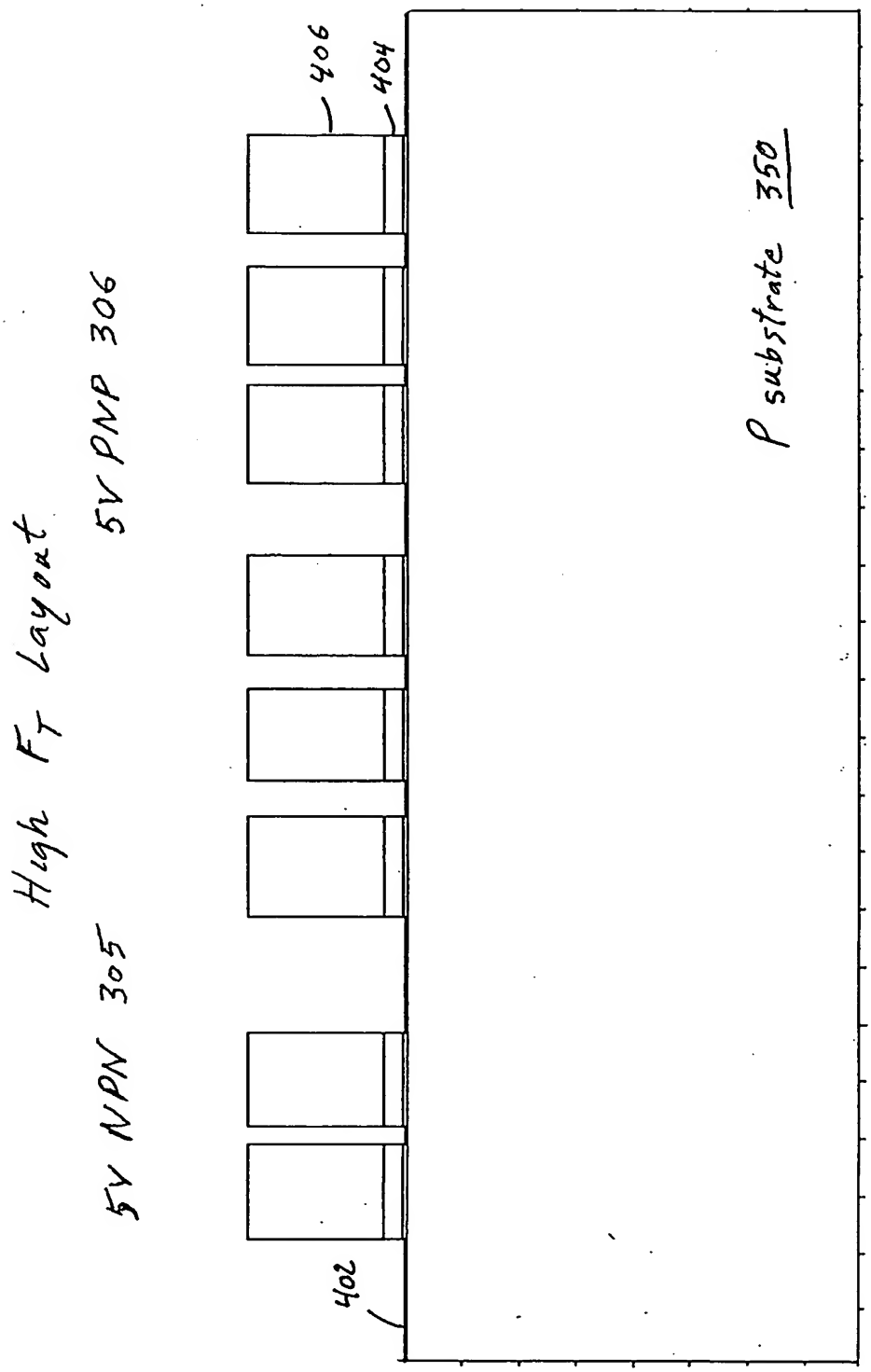

High F_T Layout
5V NPN 305
5V PNP 306
406
404
402
P substrate 350
LOCOS - Nitride Mask and Etch

Fig. 22B

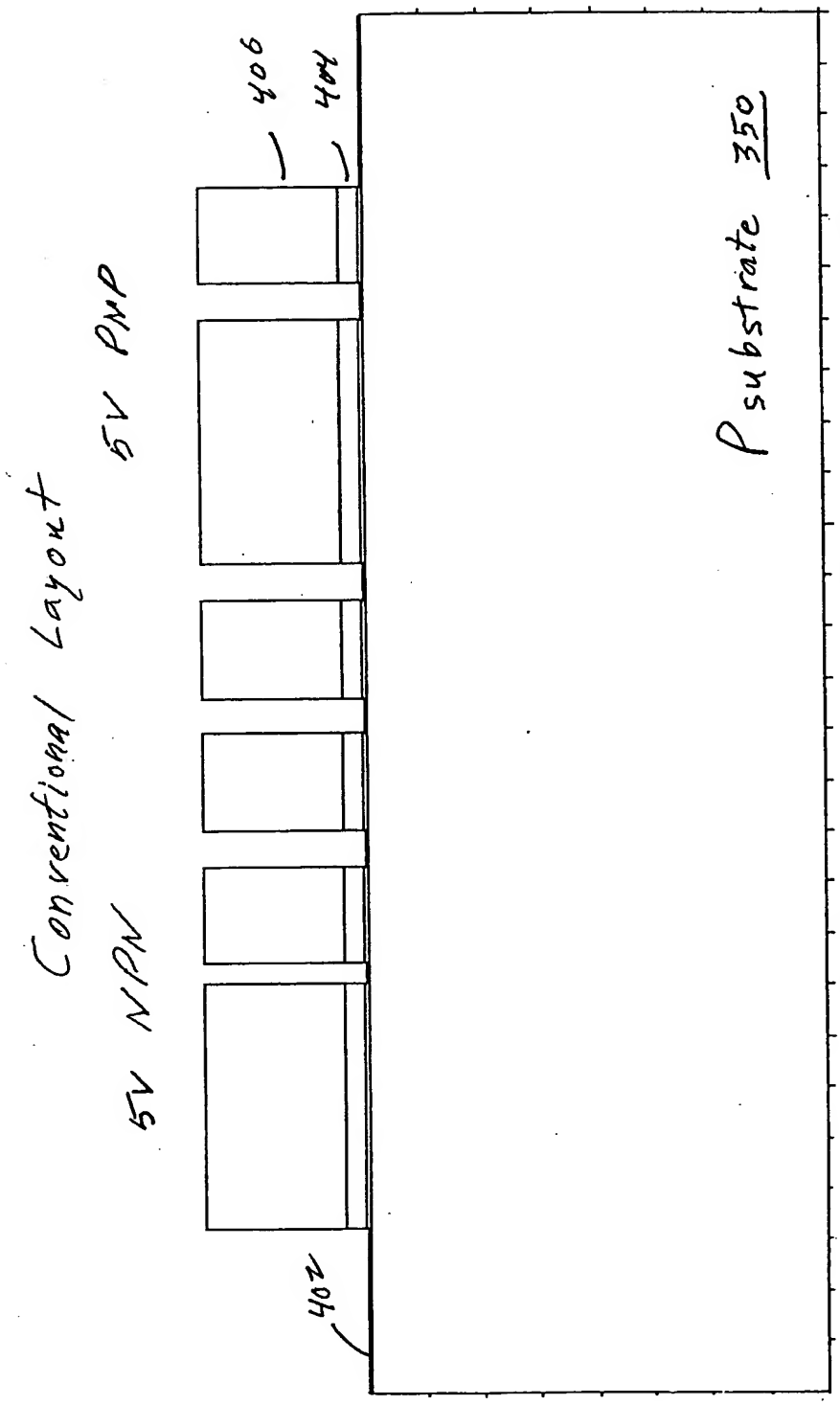

406
404
P substrate 350
LOCOS - Nitride Mask and Etch
5V PMP
5V NMN
Conventional Layout
404

Fig. 22C

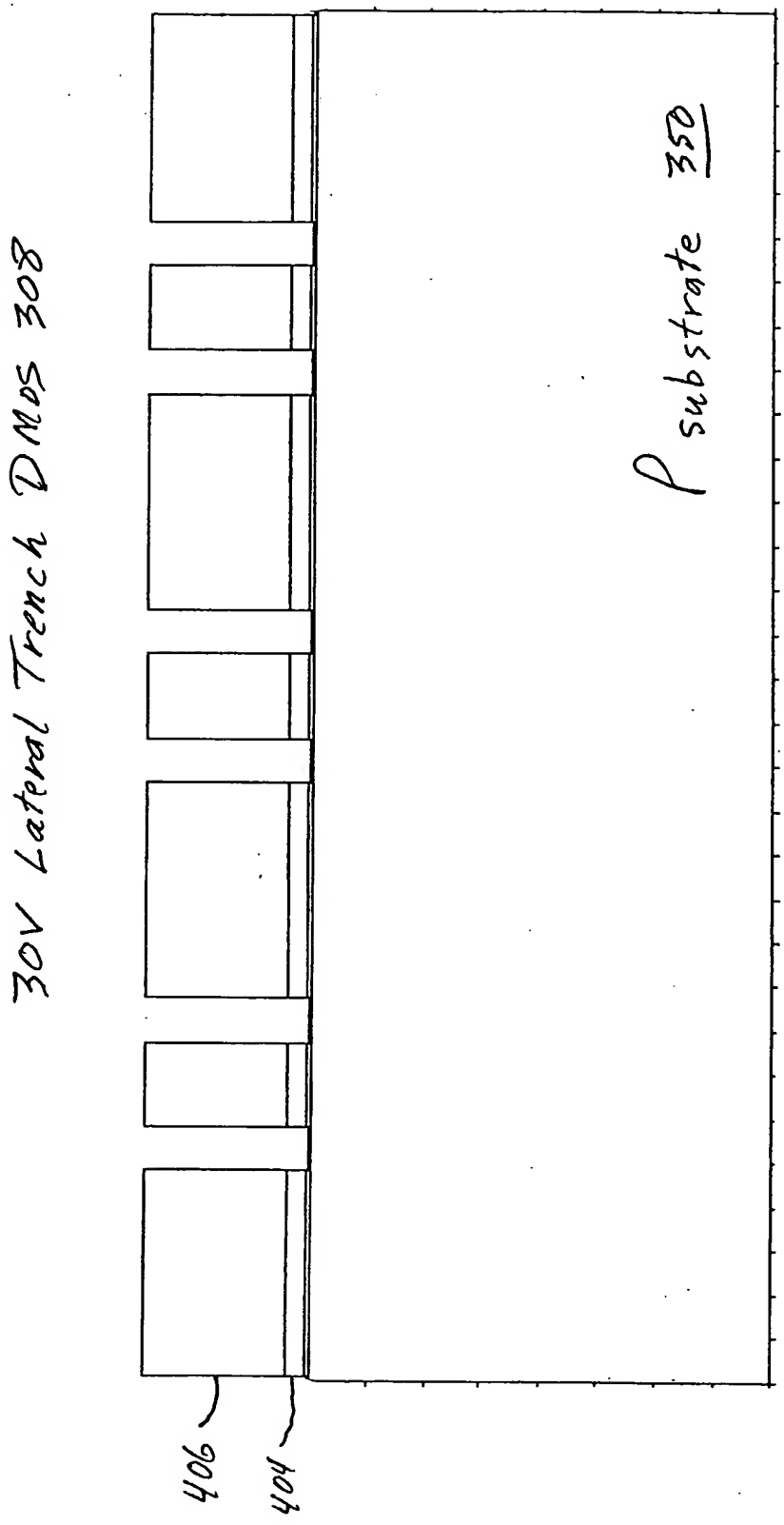
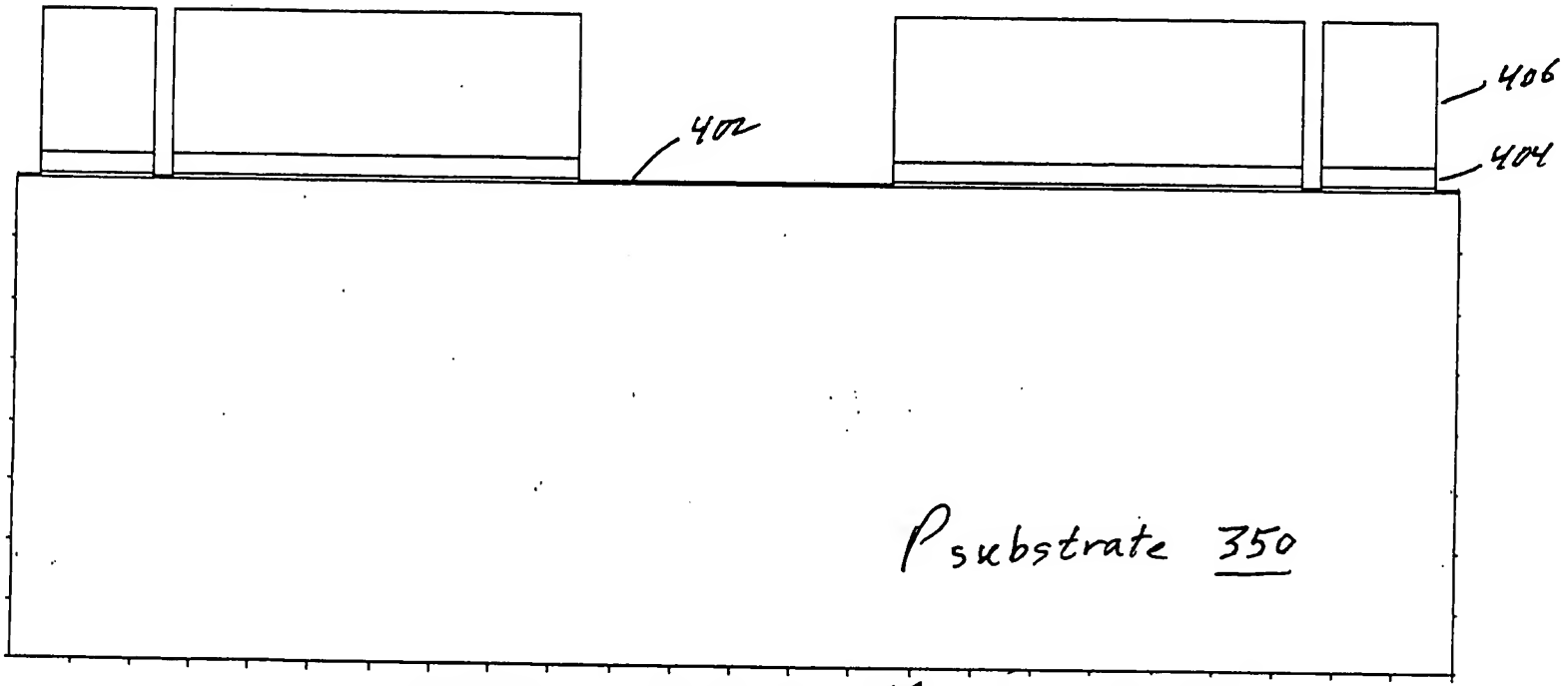

30V Lateral Trench DMos 308
P substrate 350
LOCOS - Nitride Mask and Etch
406
404

Fig. 22D

Symmetrical 12V CMOS

12V PMOS 309

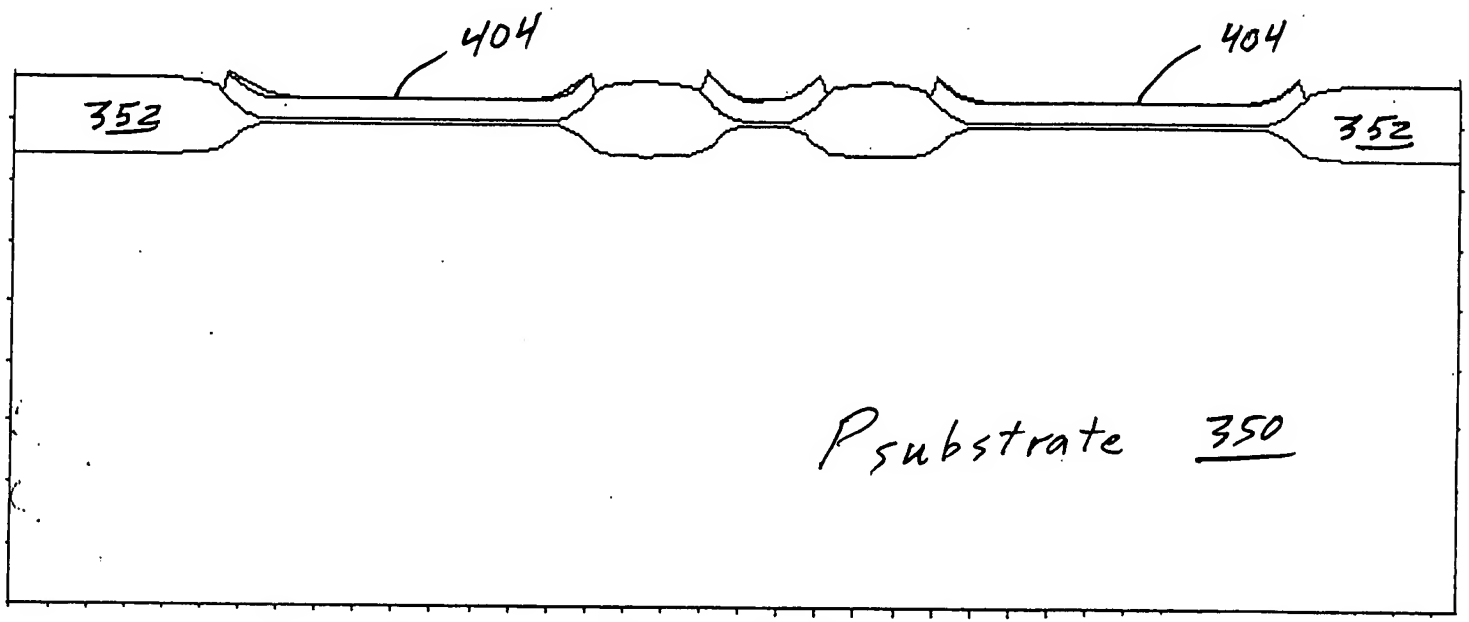
12V NMOS 310



LOCOS - Nitride Mask and Etch

Fig. 22E

5V PMOS 301 5V NMOS 302



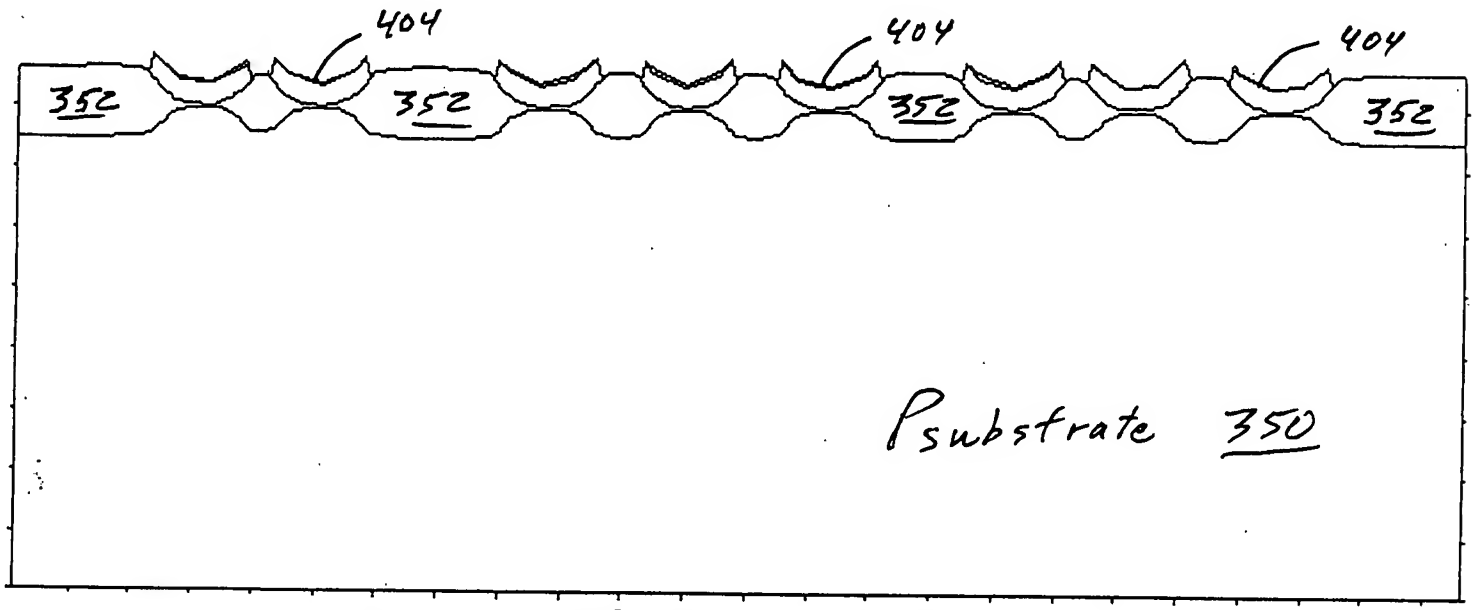
LOCOS – Field Oxidation

Fig. 23A

High F_T Layout

5V NPN 305

5V PNP 306

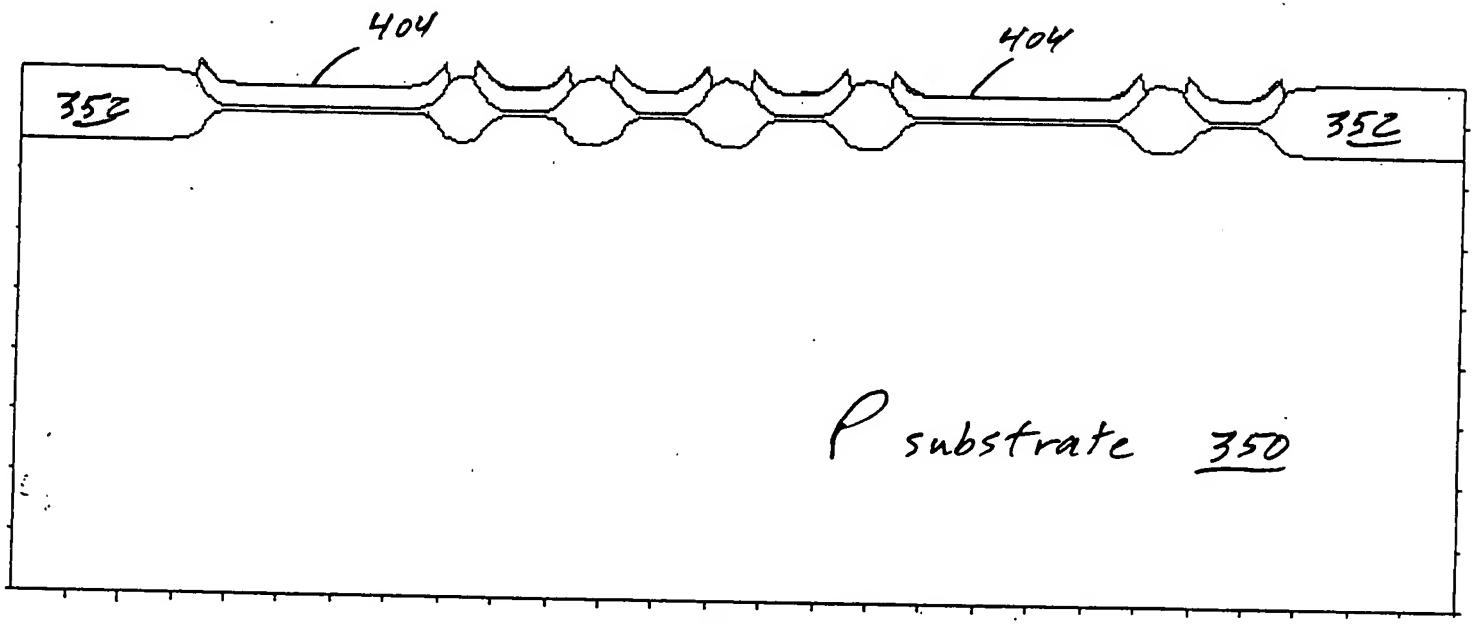


LOCOS - Field Oxidation

Fig. 23B

Conventional Layout

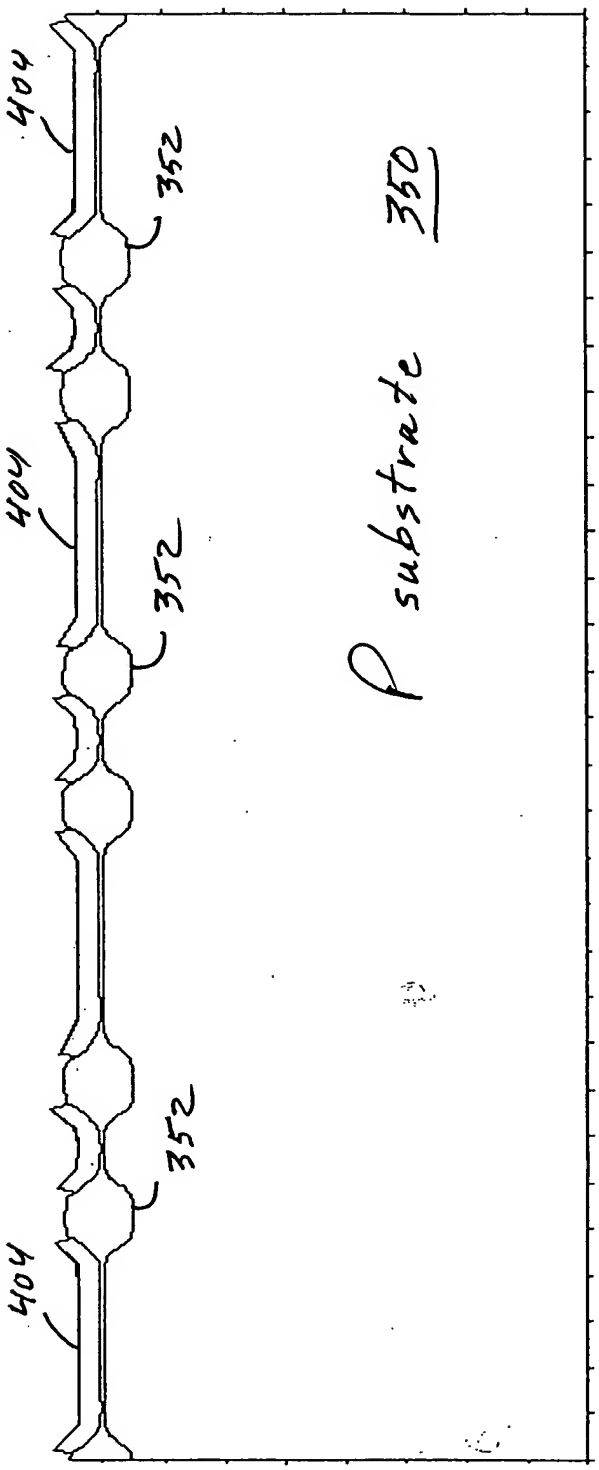
5V NPN 5V PNP



LOCOS - Field Oxidation

Fig 23C

30V Lateral Trench DMOS

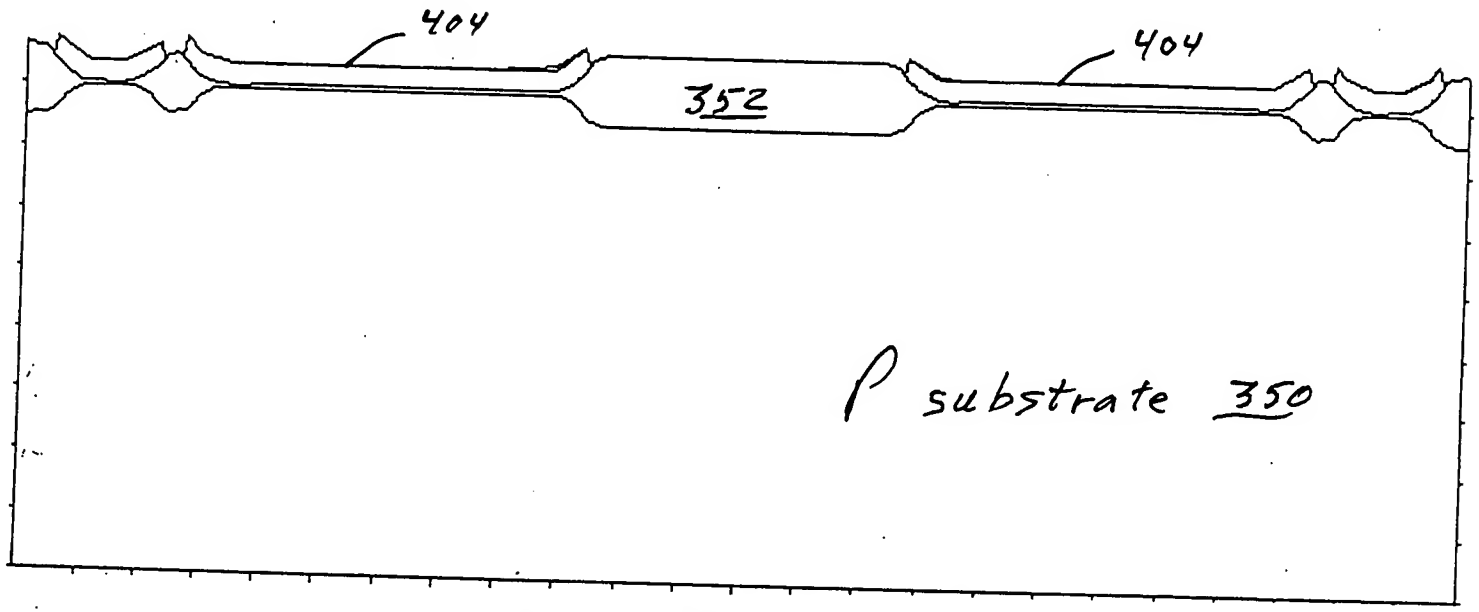


LOCOS - Field Oxidation

Fig. 23D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



LOCOS - Field Oxidation

Fig. 23E

5V PMOS 301

5V NMOS 302

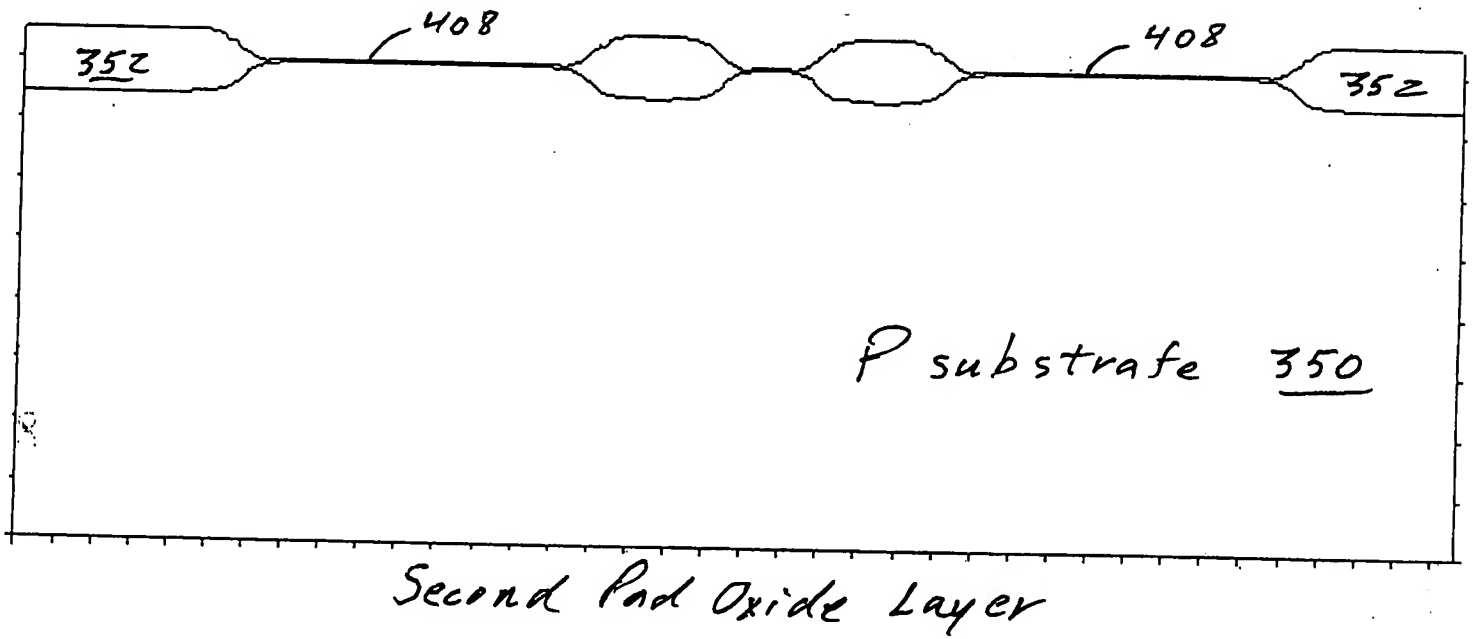


Fig. 24A

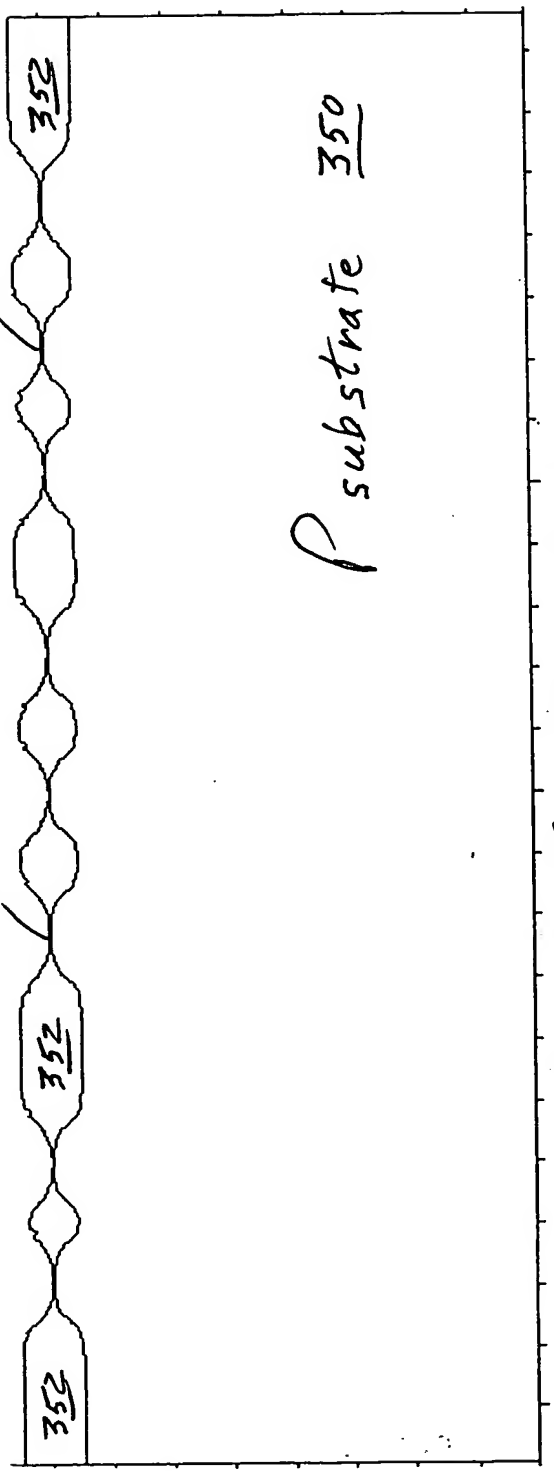
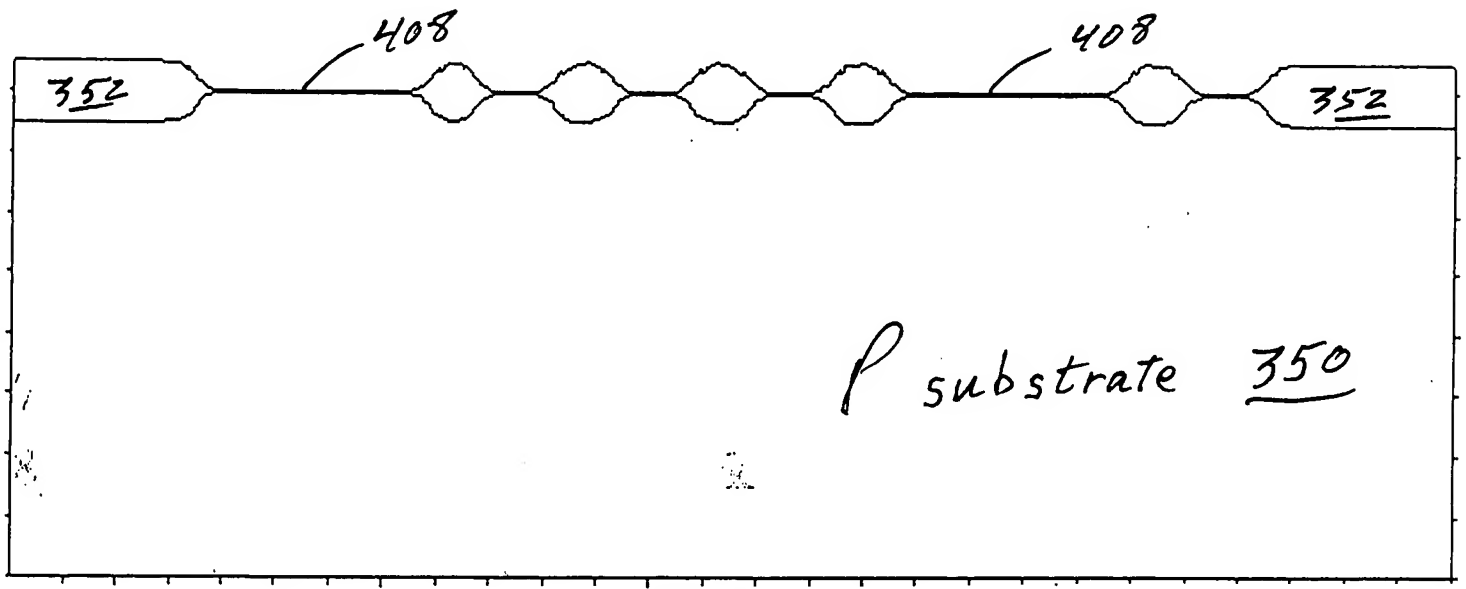

High F_T Layout
5V NPN 305
5V PNP 306
352
352
352
408
408
P substrate 350
Second Pad Oxide Layer

Fig. 24B

Conventional Layout

5V NPN

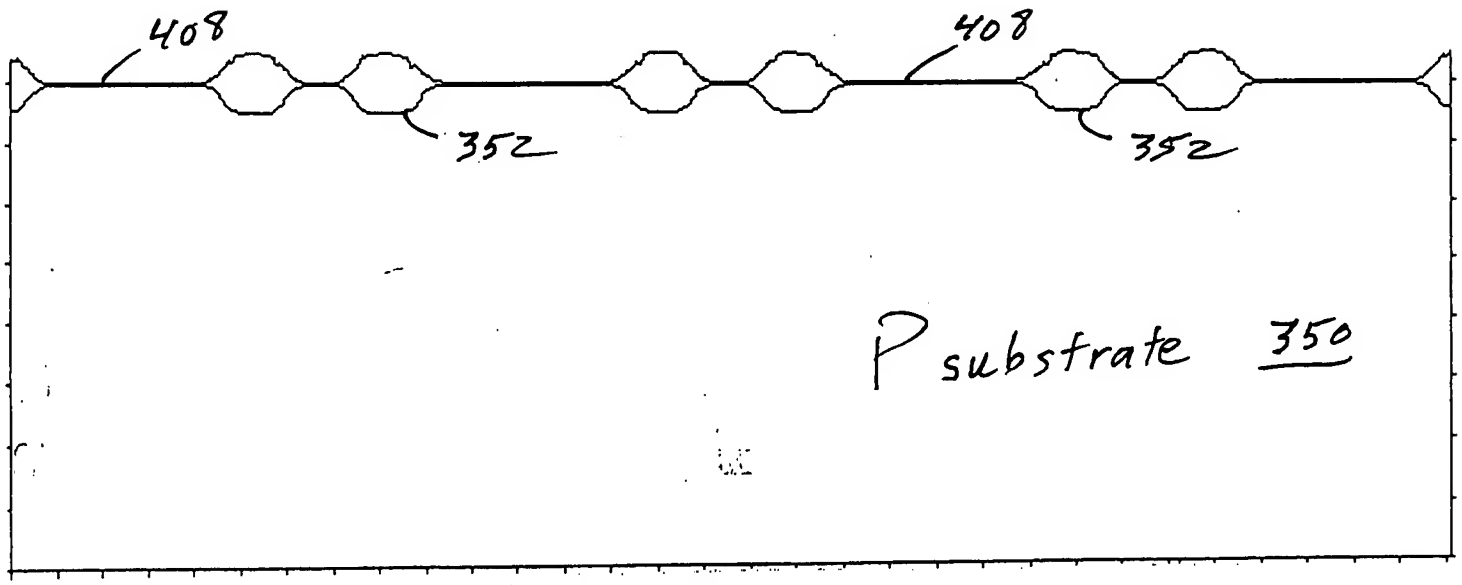
5V PNP



Second Pad Oxide Layer

Fig. 24C

30V Lateral Trench DMOS 308

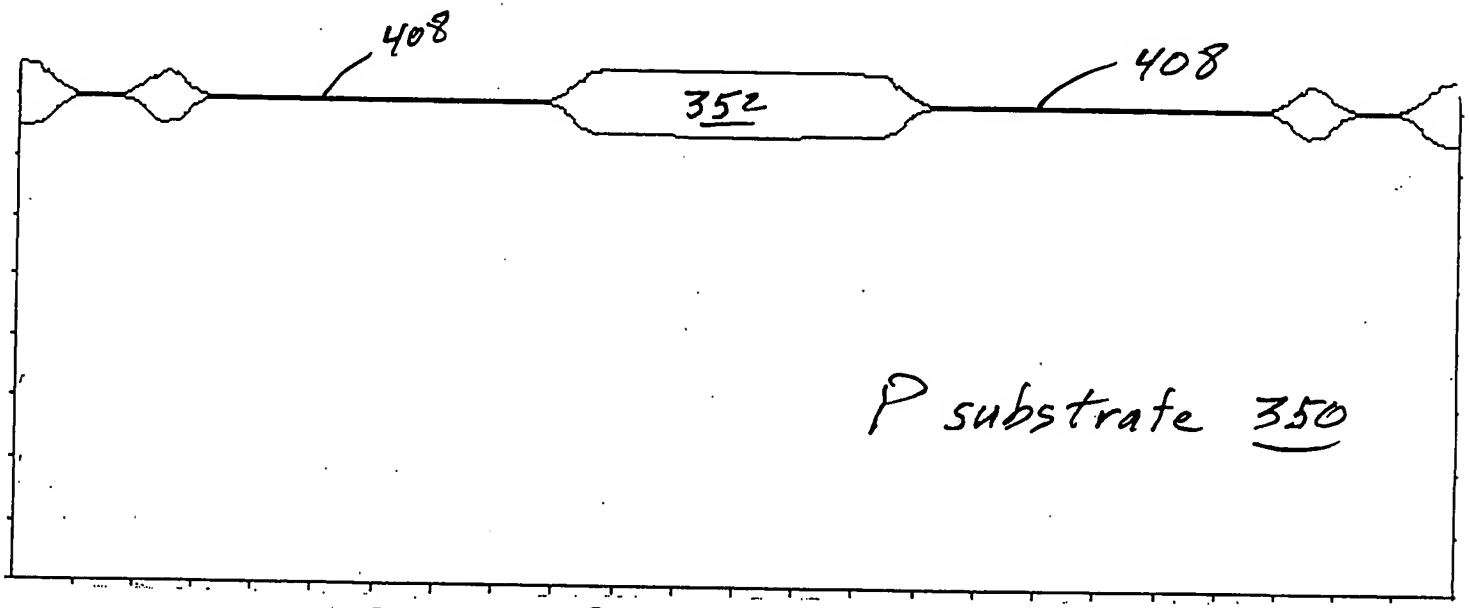


Second Pad Oxide Layer

Fig. 24D

Symmetrical 12V CMOS

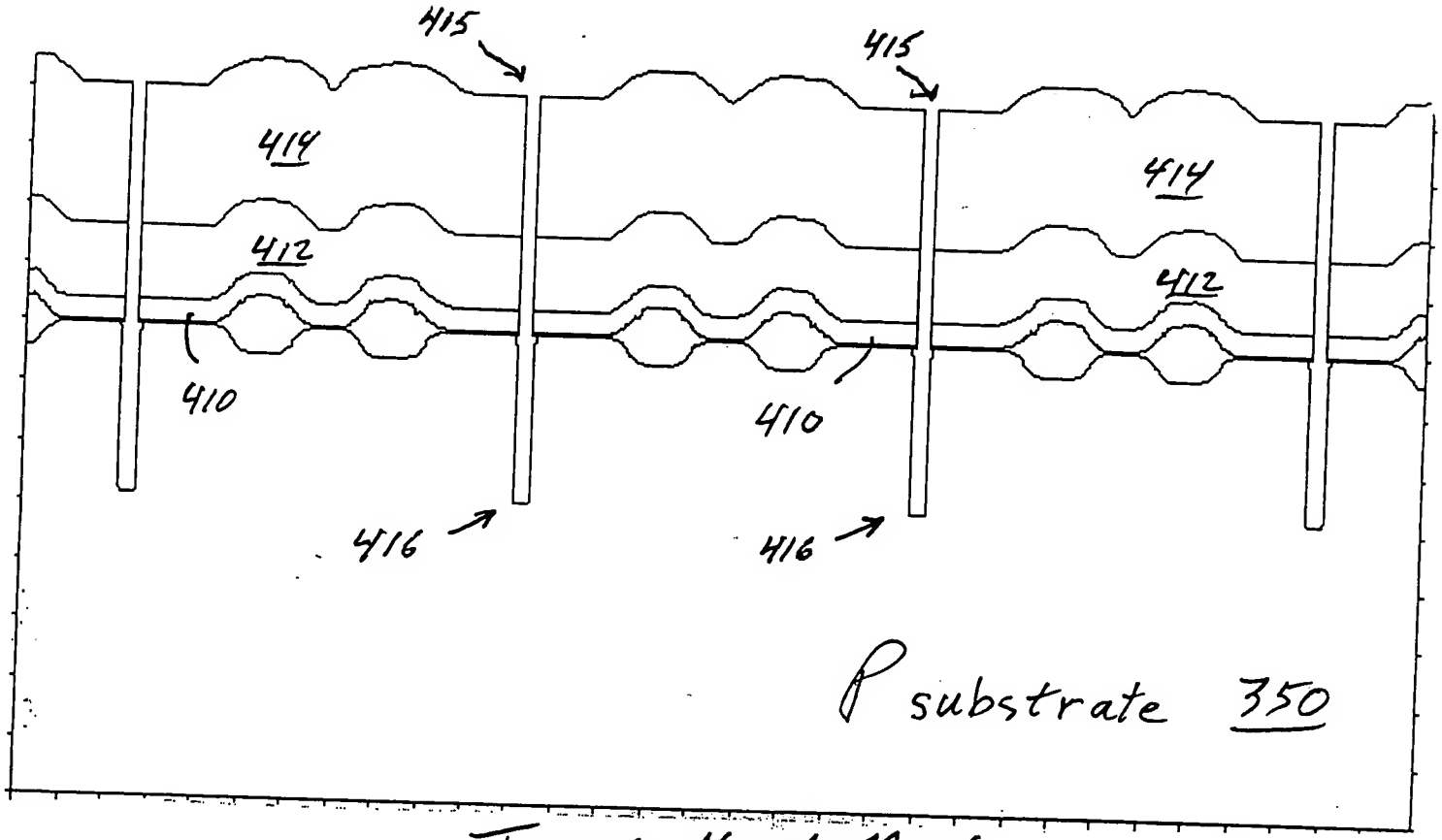
12V PMOS 309 12V NMOS 310



Second Pad Oxide Layer

Fig. 24E

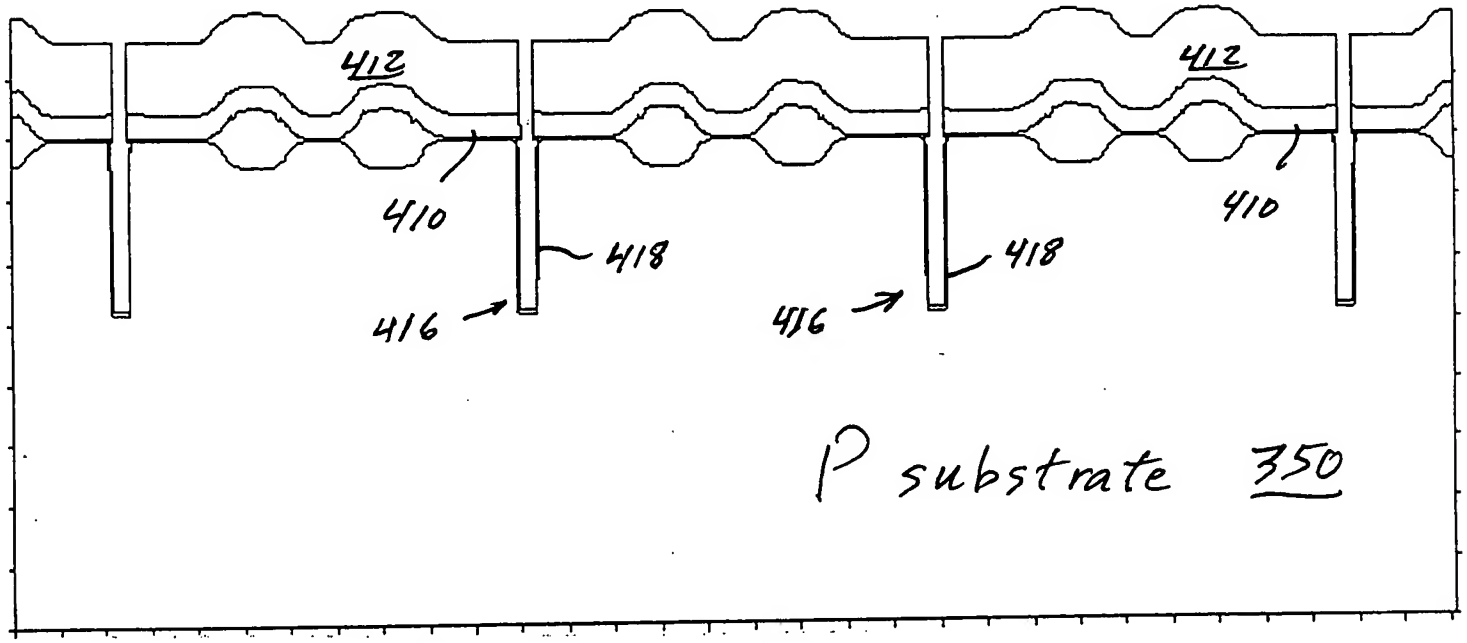
30V Lateral Trench DMOS 308



Trench Hard Mask

Fig. 25D

30V Lateral Trench DMOS 308



Sacrificial Oxide

Fig. 26D

30 V Lateral Trench DMOS 308

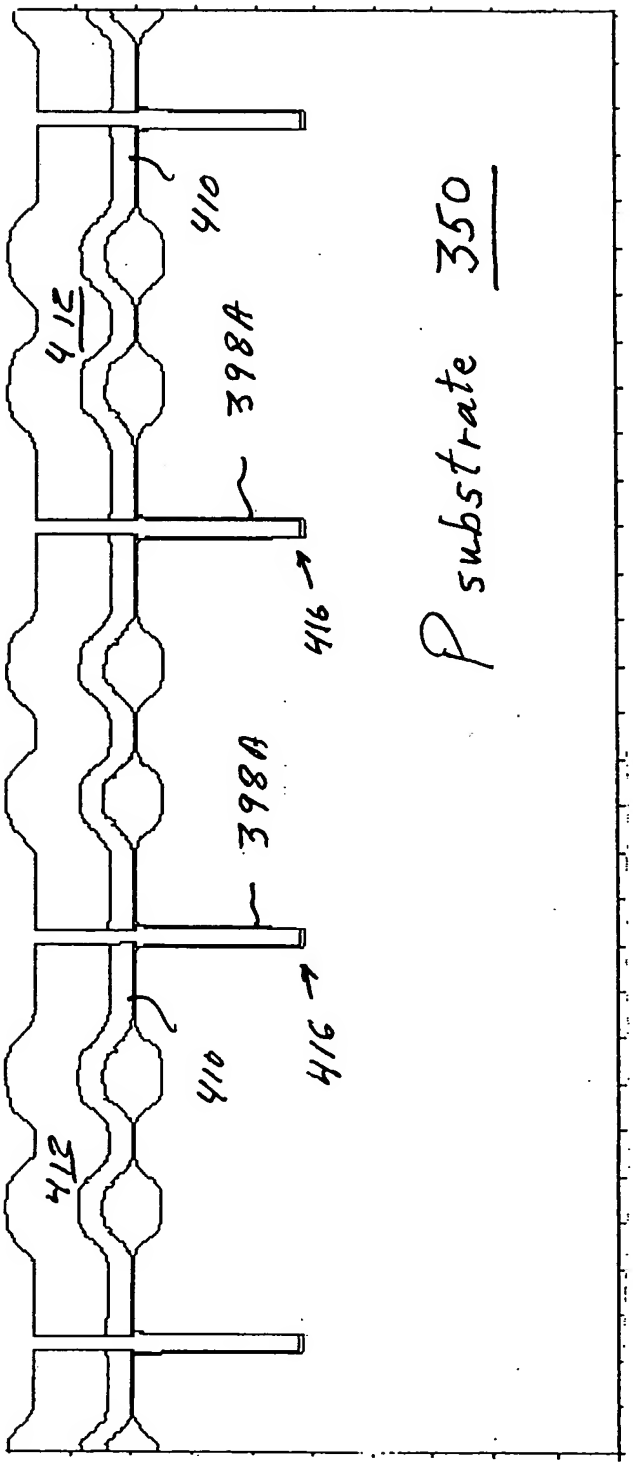
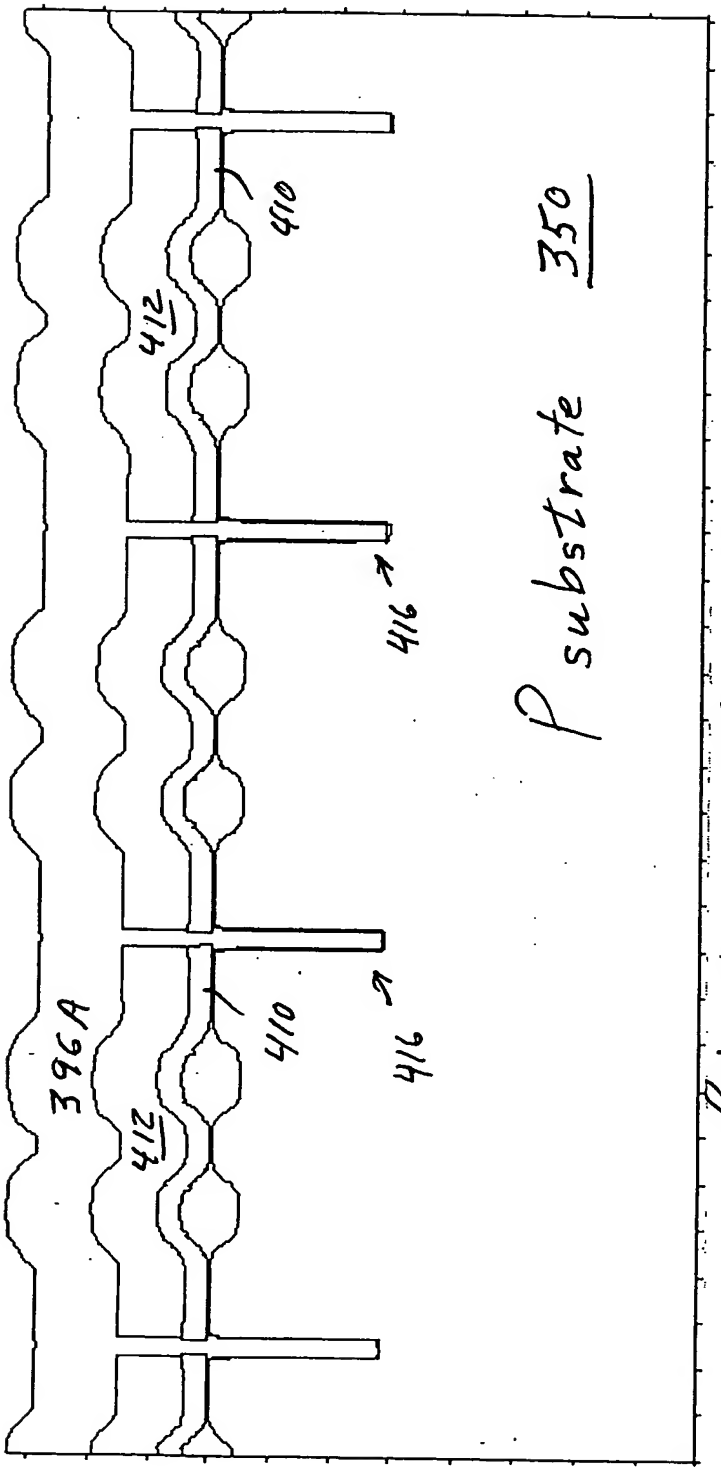


Fig. 27D

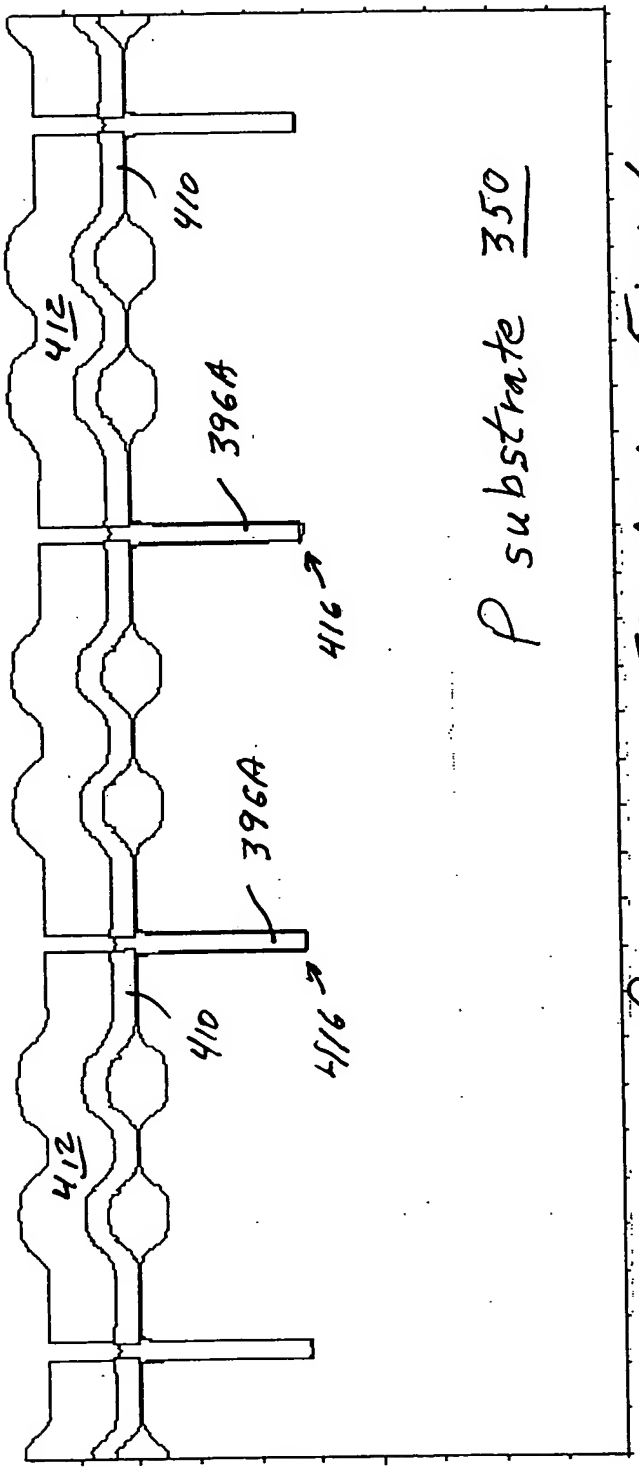
30 V Lateral Trench DMOS 308



Polysilicon - First Layer

Fig 28D

30V Lateral Trench DMOS 308



Polysilicon Etchback - First Layer

Fig. 29D

30V Lateral Trench DMOS 308

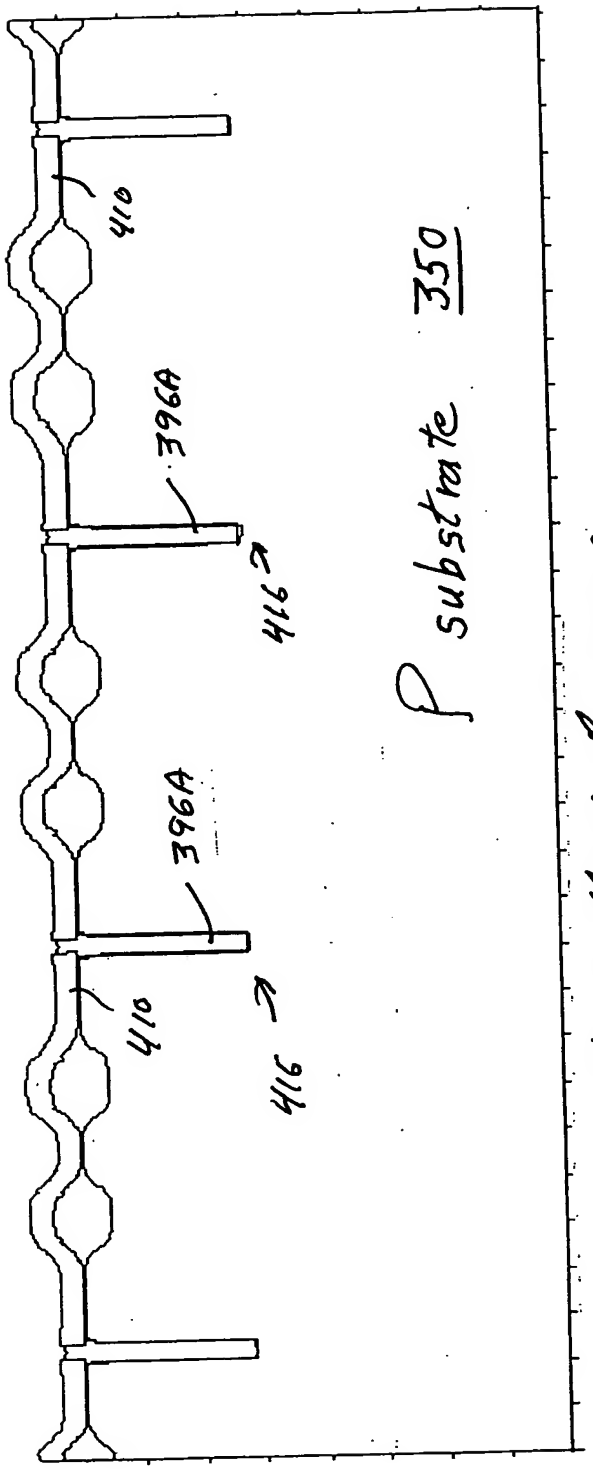
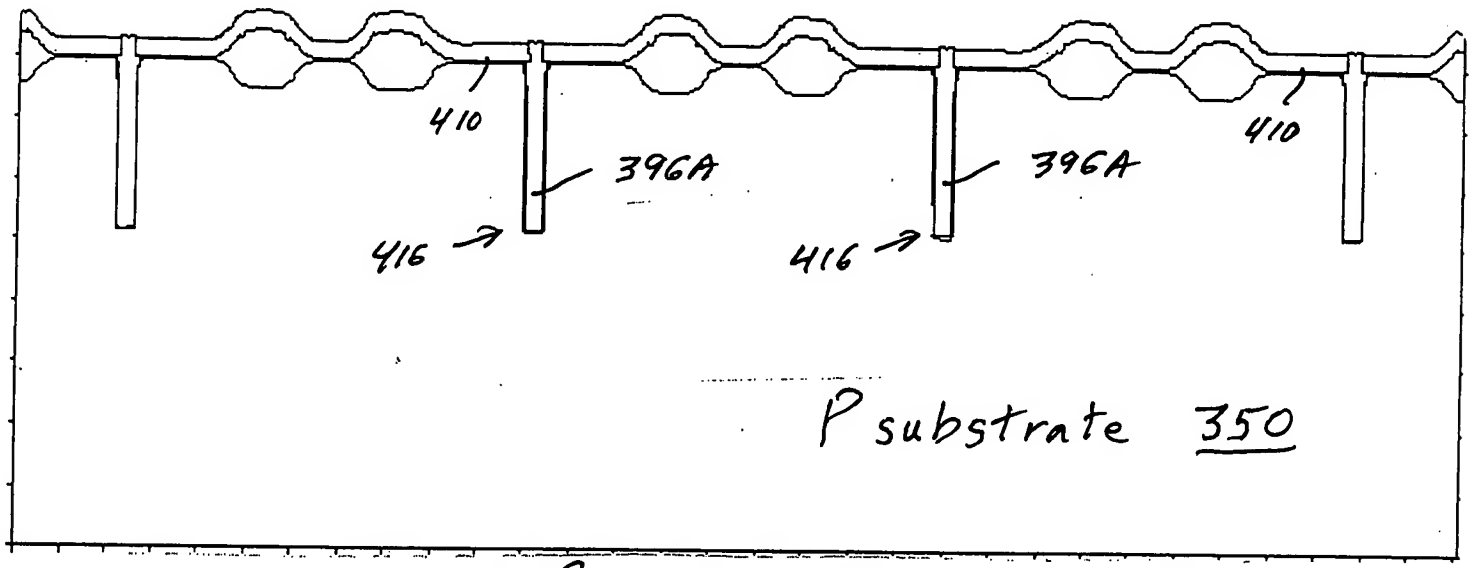


Fig. 30D

- 30V Lateral Trench DMOS 308



Second Polysilicon Etchback – First Layer

Fig. 31D

30V Lateral Trench DMOS 308

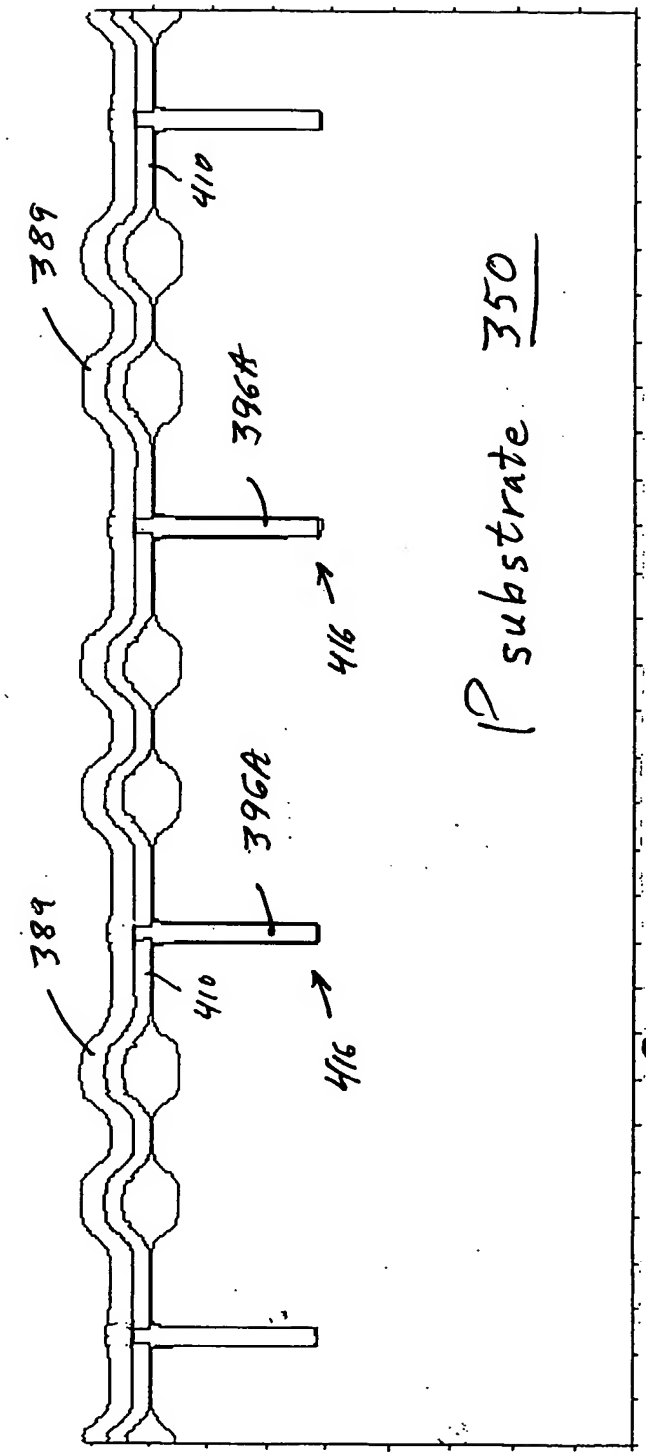
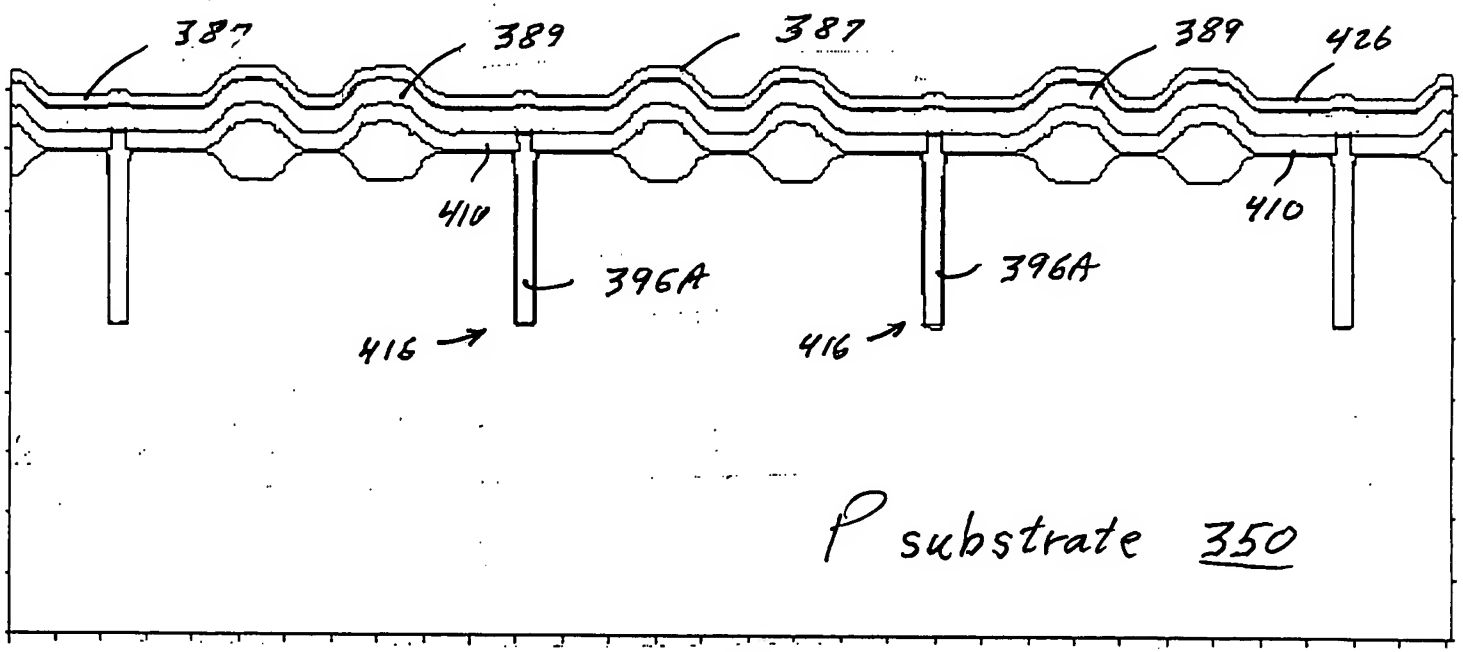


Fig. 32D

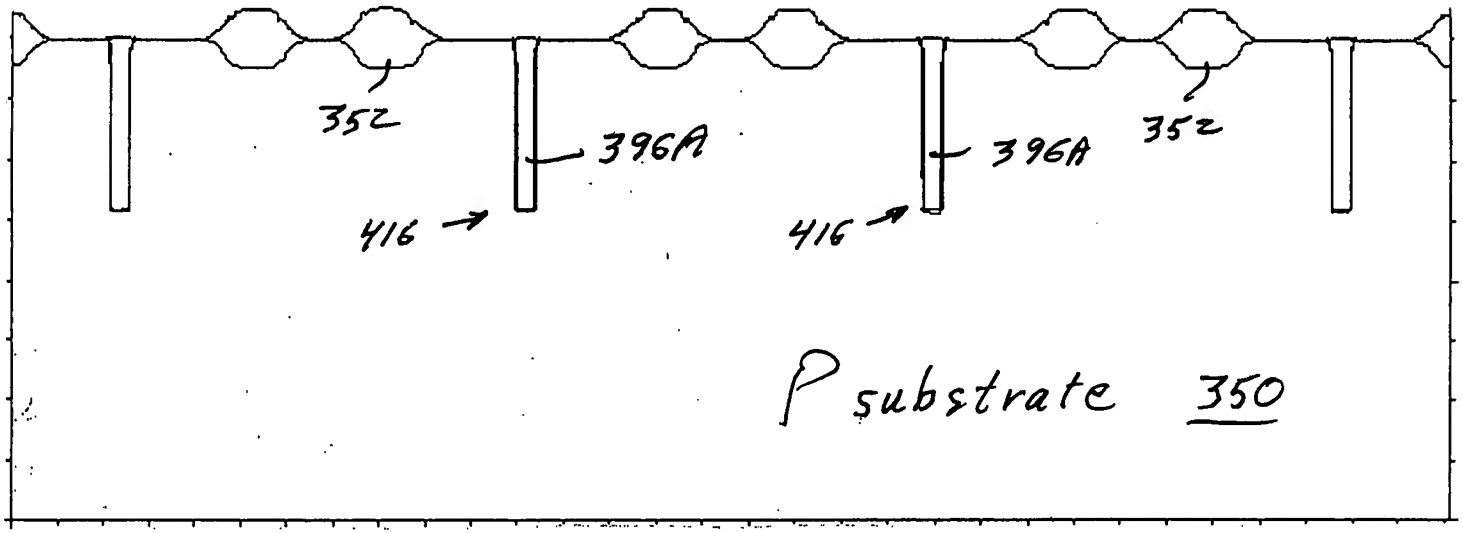
30V Lateral Trench DMOS 308



Interlayer Dielectric

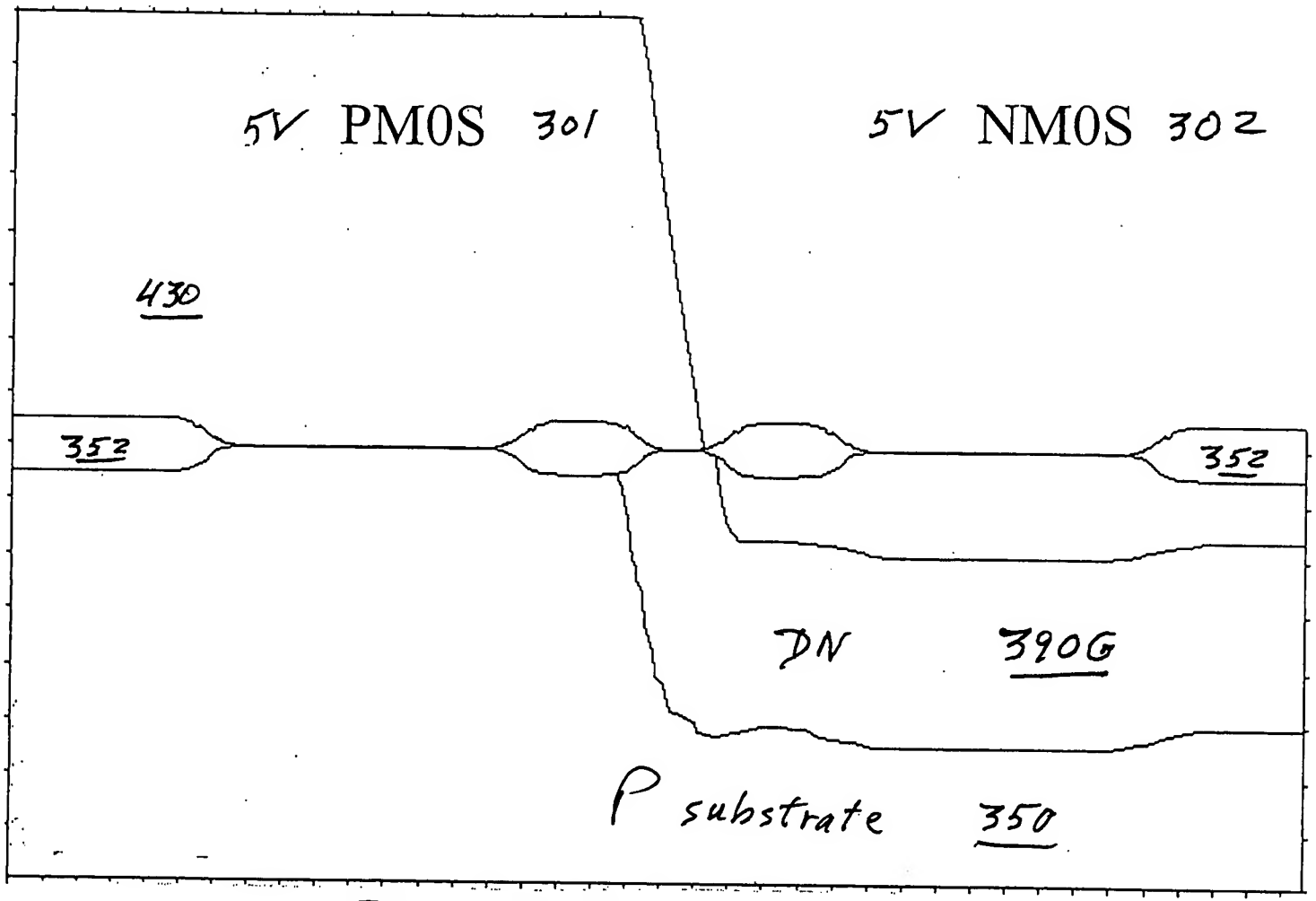
Fig 33D

30 V Lateral Trench DMOS 308



Etchback - Interlayer Dielectric and Second Poly

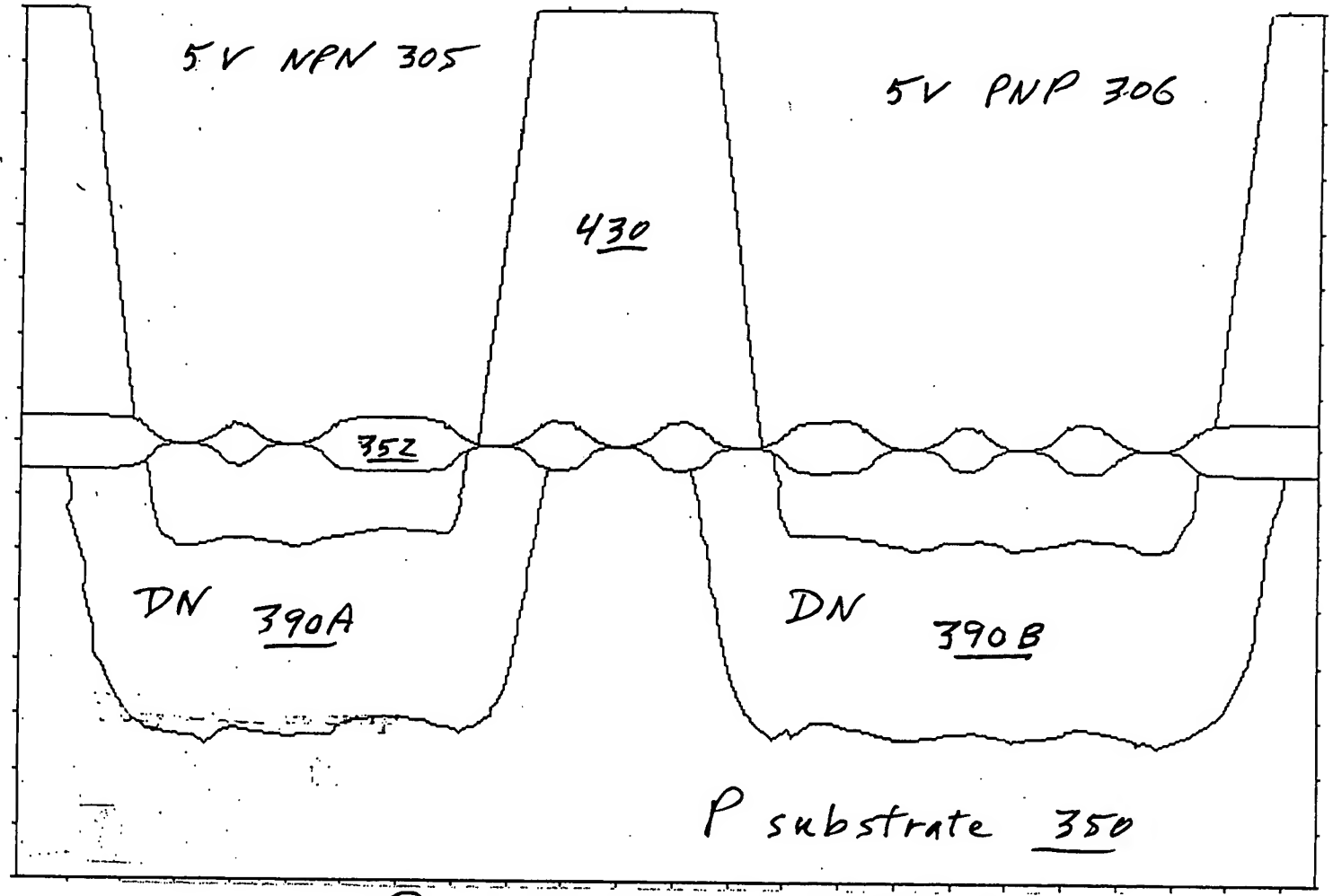
Fig. 34D



Deep N Mask and Implant

Fig. 35A

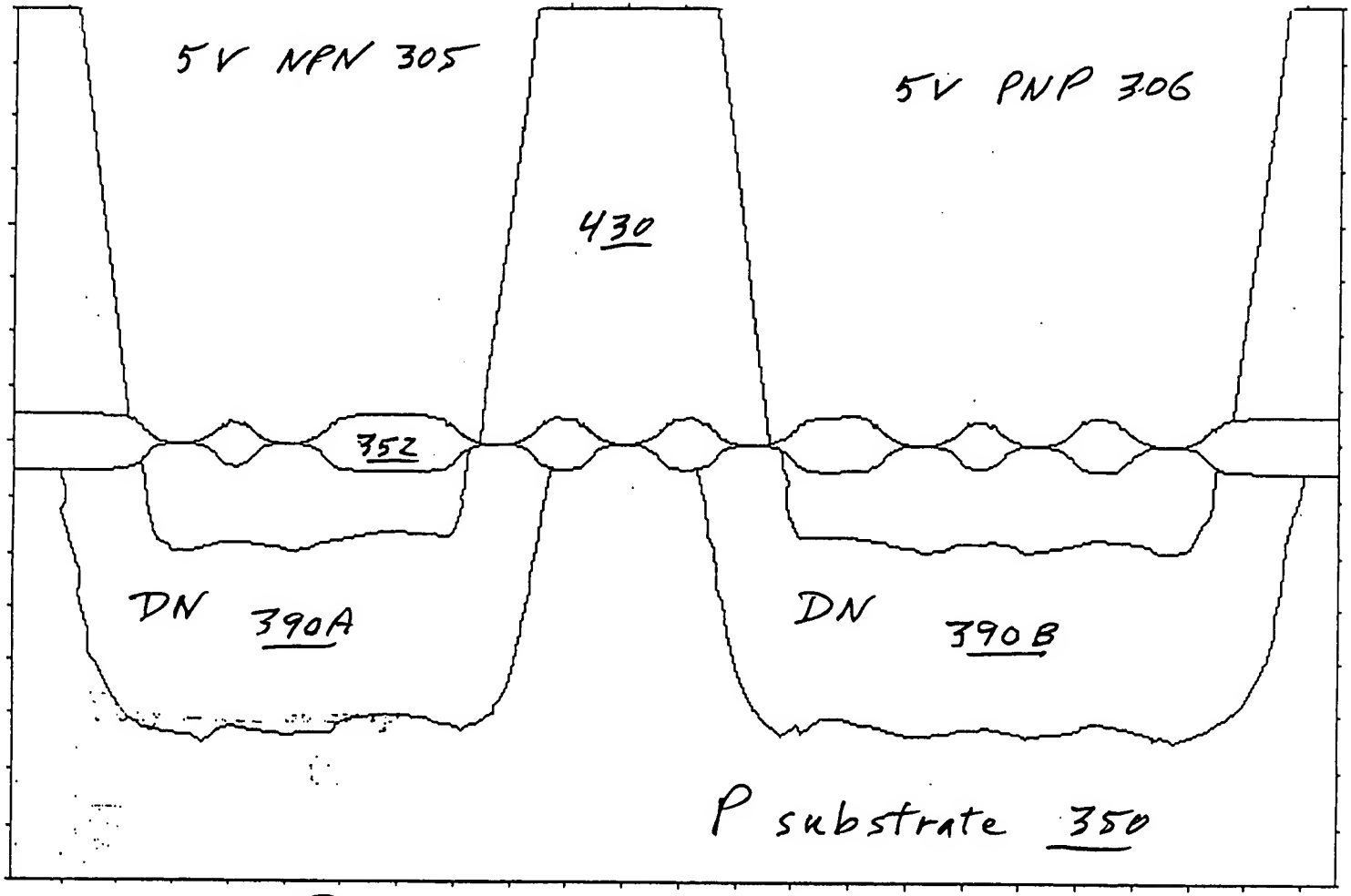
High F_T Layout



Deep N Mask and Implant

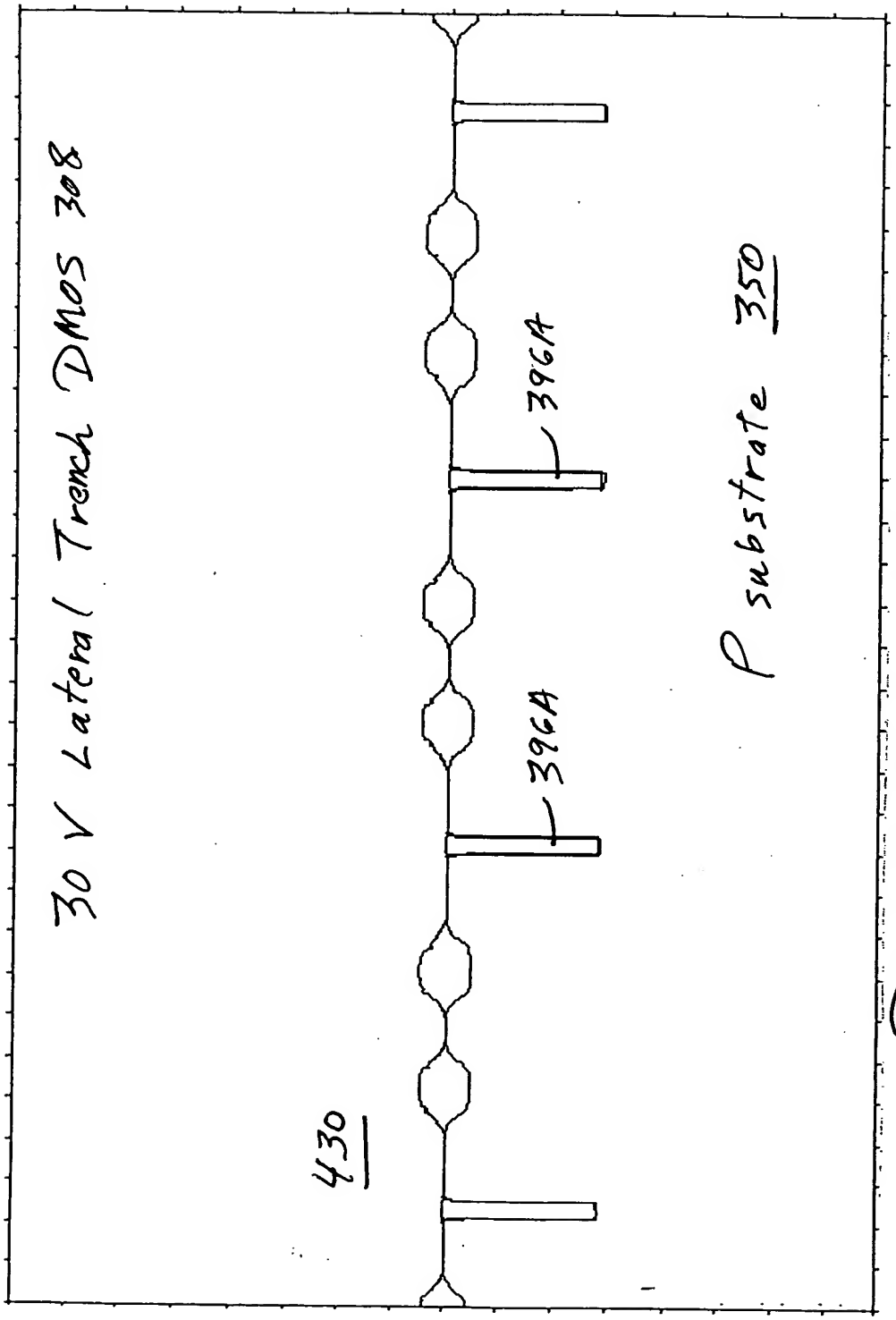
Fig 35B

Conventional Layout

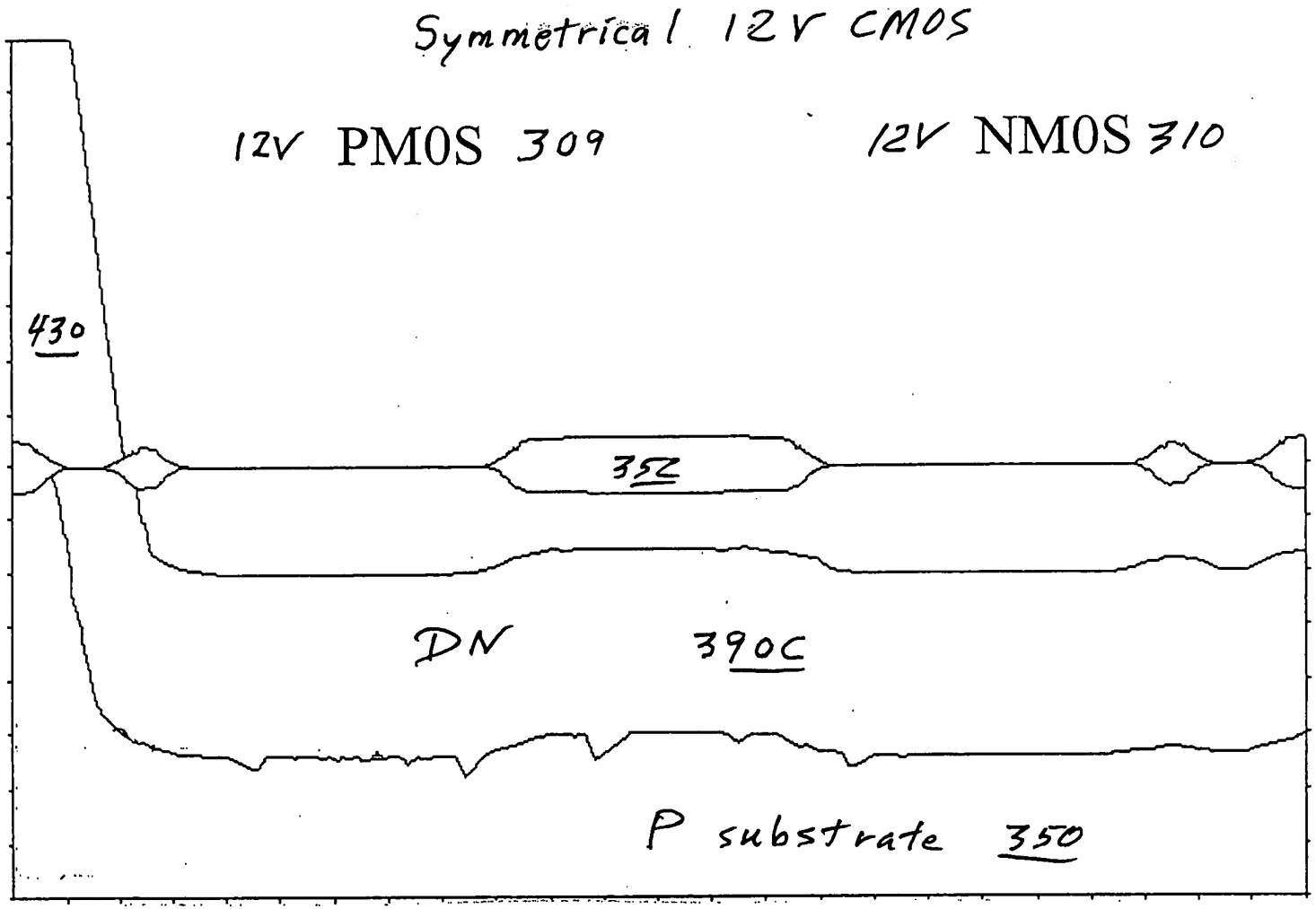


Deep N Mask and Implant

Fig. 35C



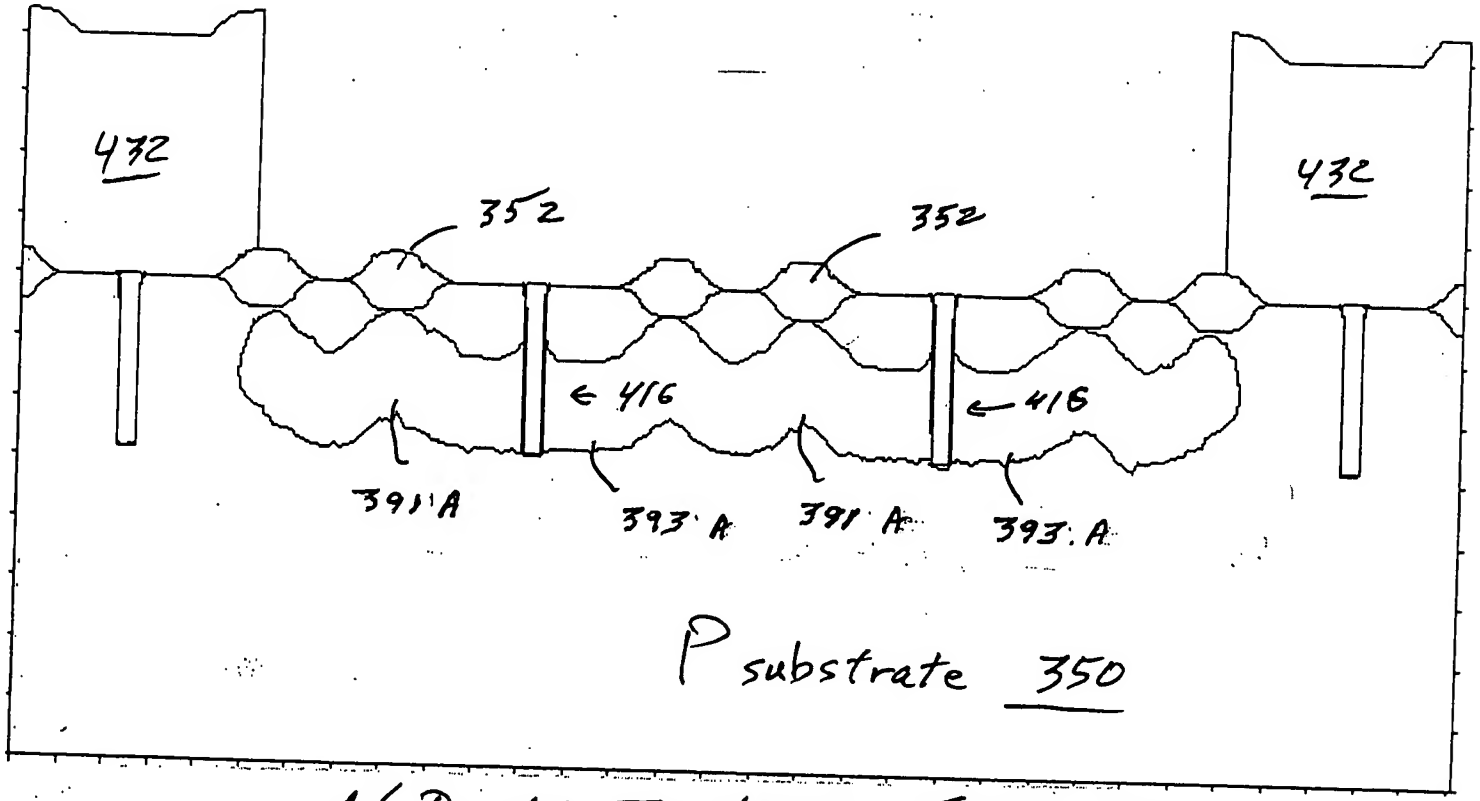
Deep N Mask and Implant
Fig. 35D



Deep N Mask and Implant

Fig. 35E

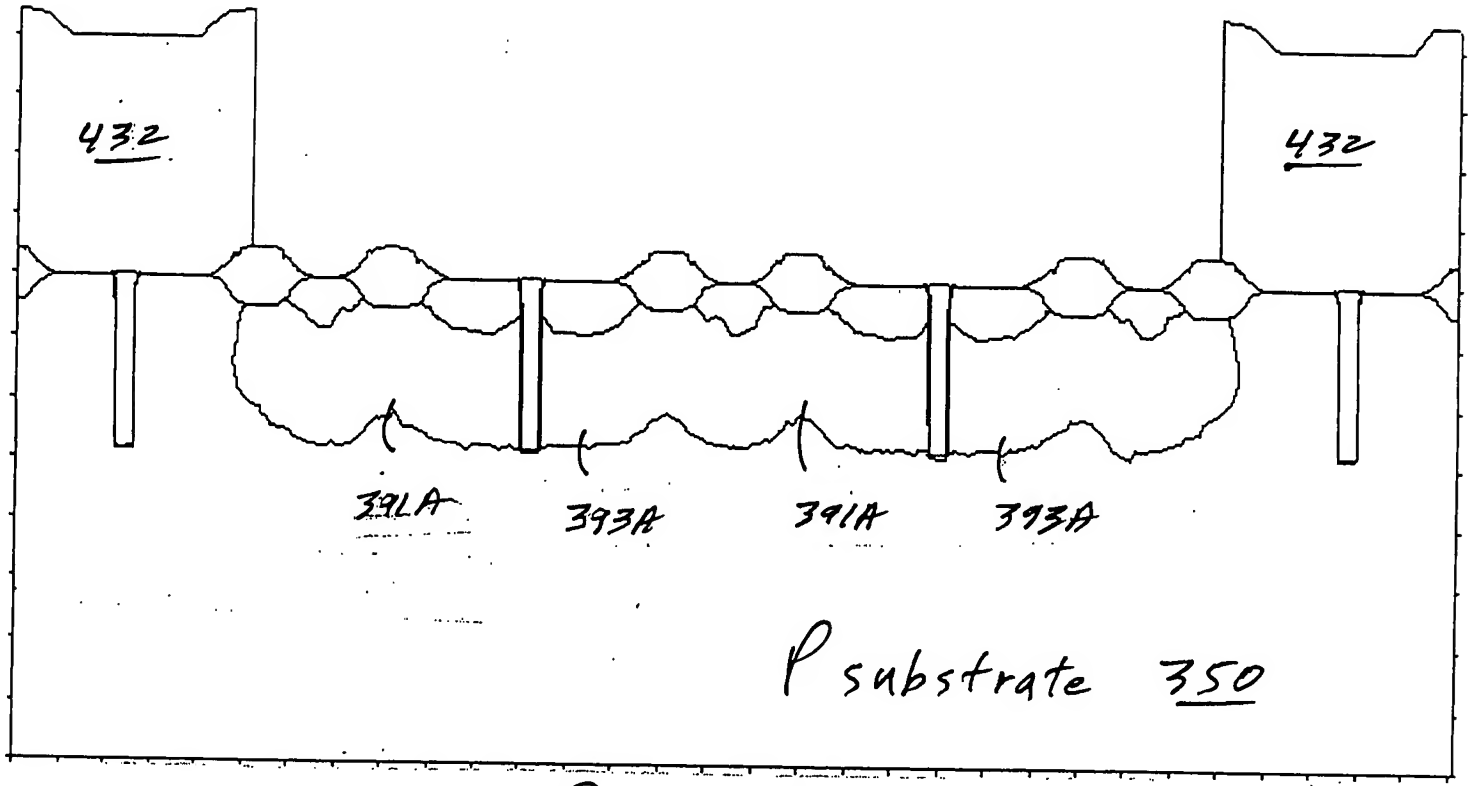
30 V Lateral Trench DMOS 308



N Drift Implant - First Stage

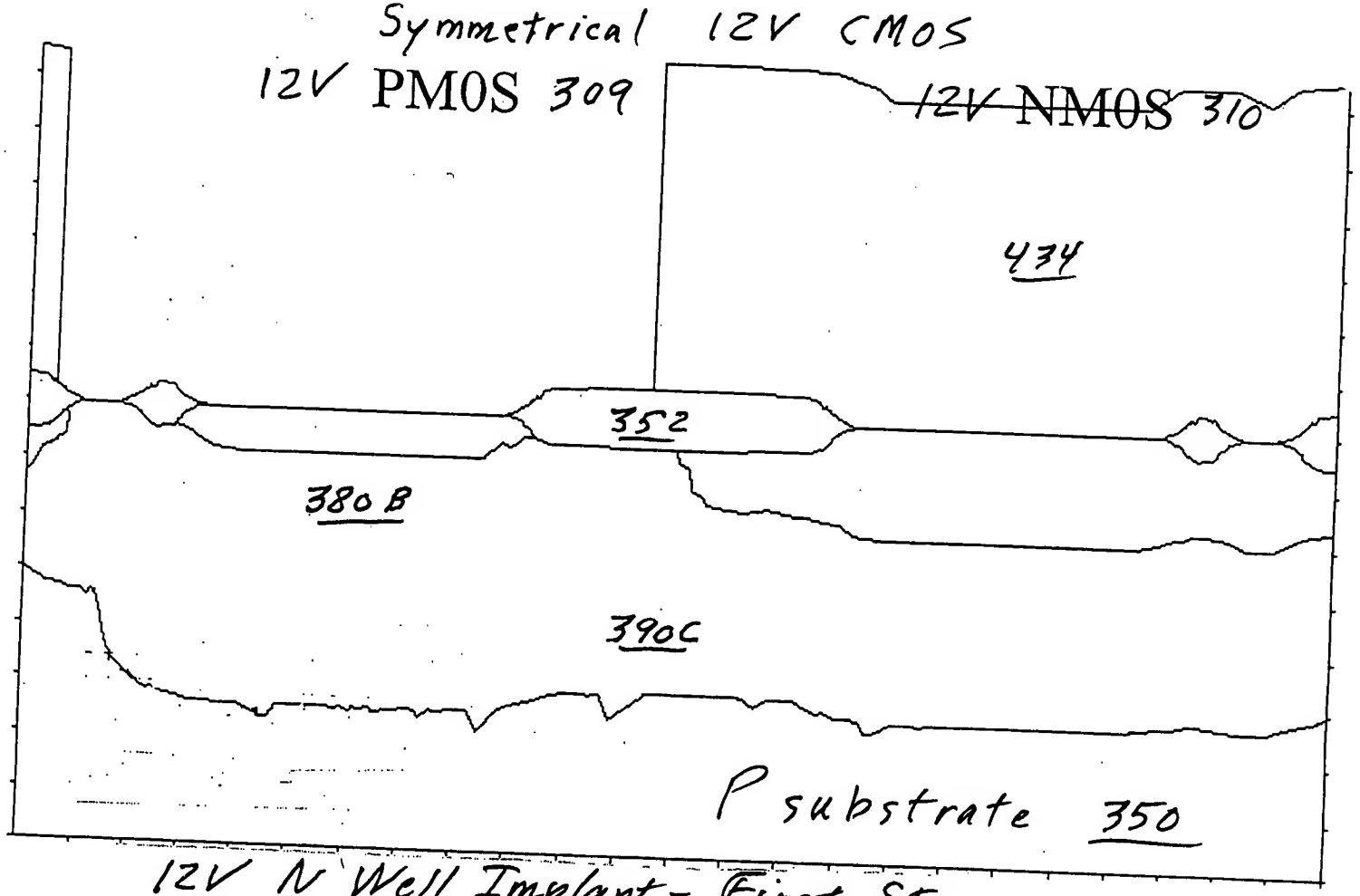
Fig. 36D

30 V Lateral Trench DMOS 308



N Drift Implant - Second Stage

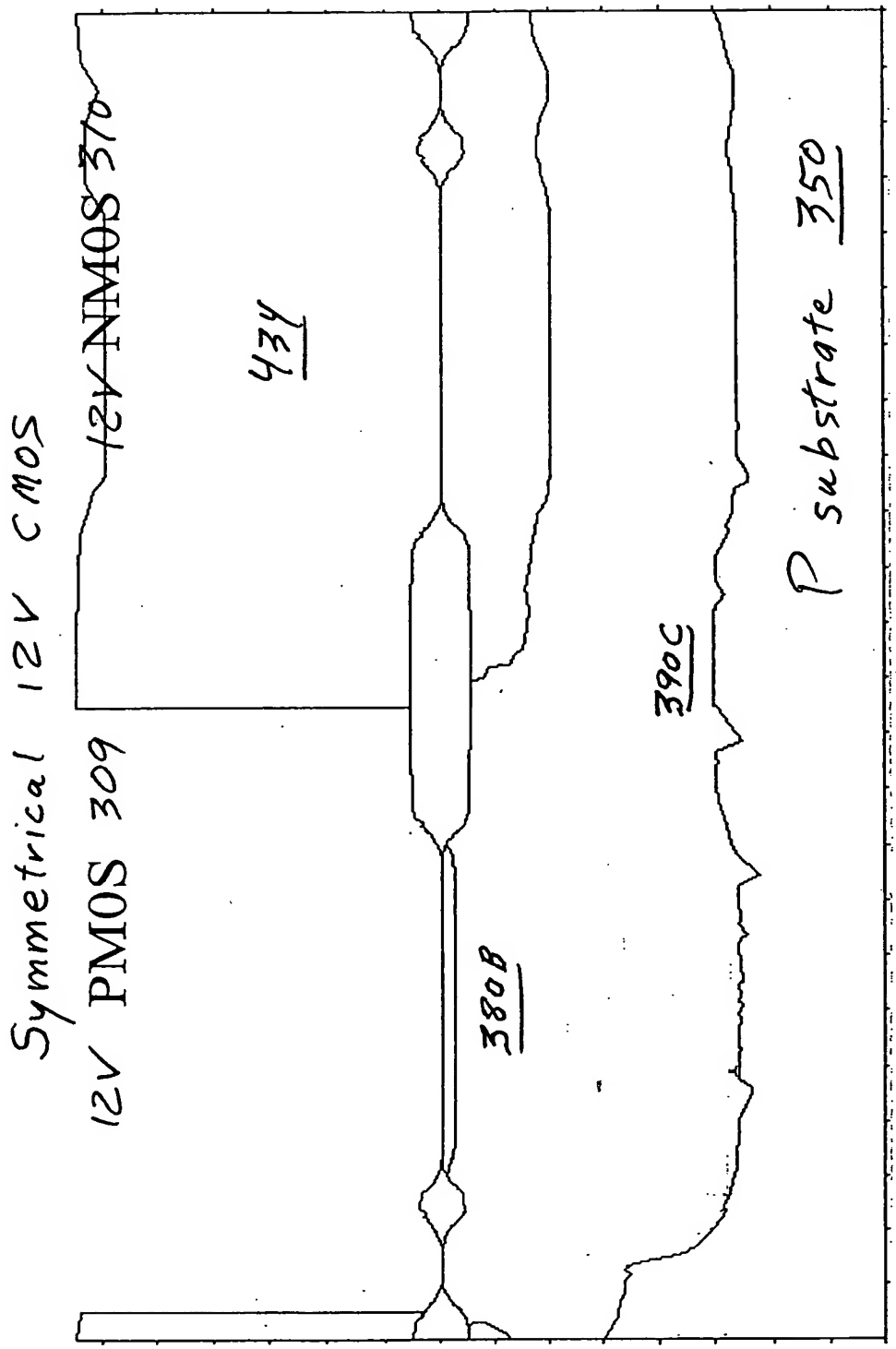
Fig. 37D



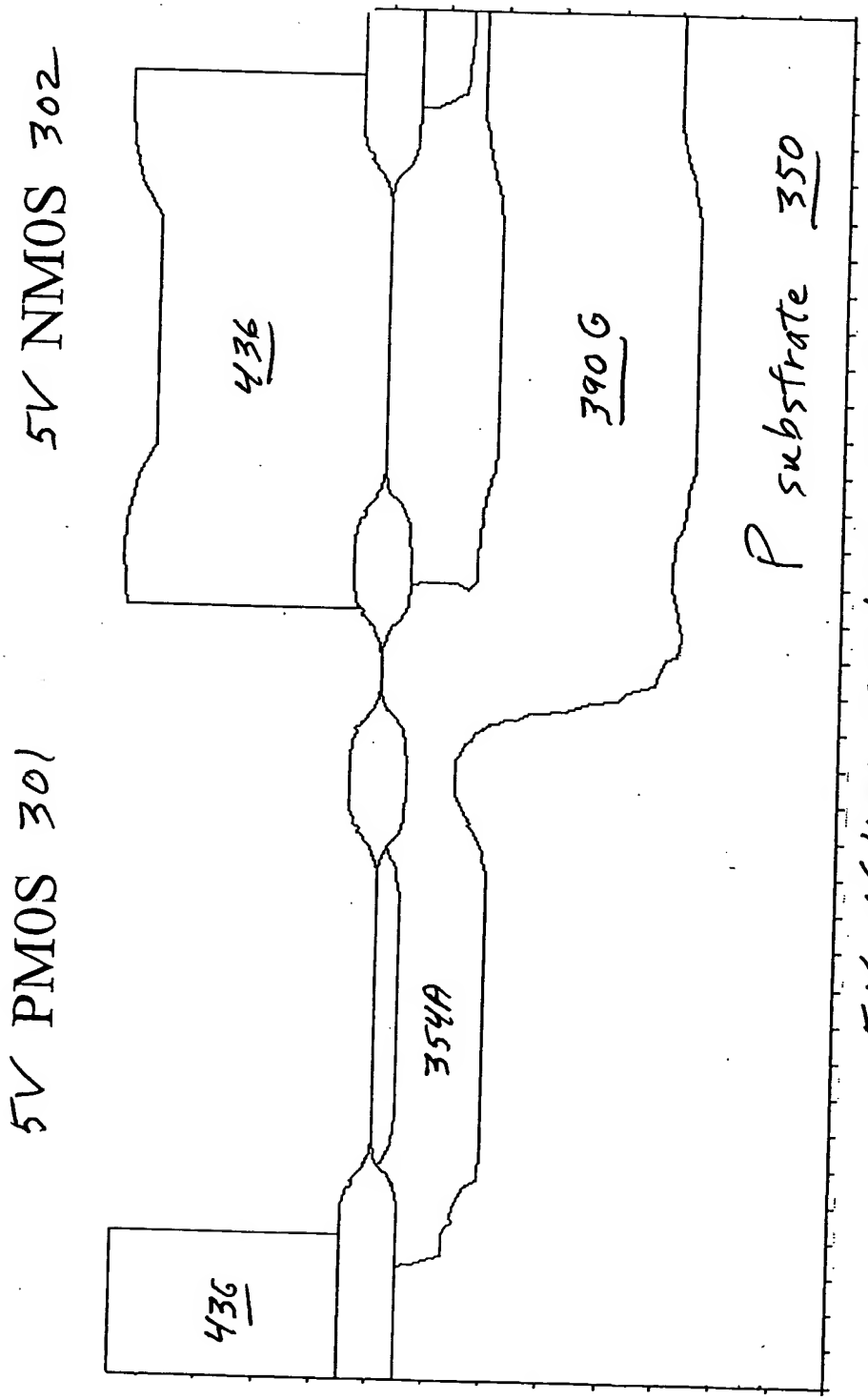
12V N Well Implant - First Stage

Fig. 38E

6/12/11



12V N Well Implant - Second Stage
Fig. 39E



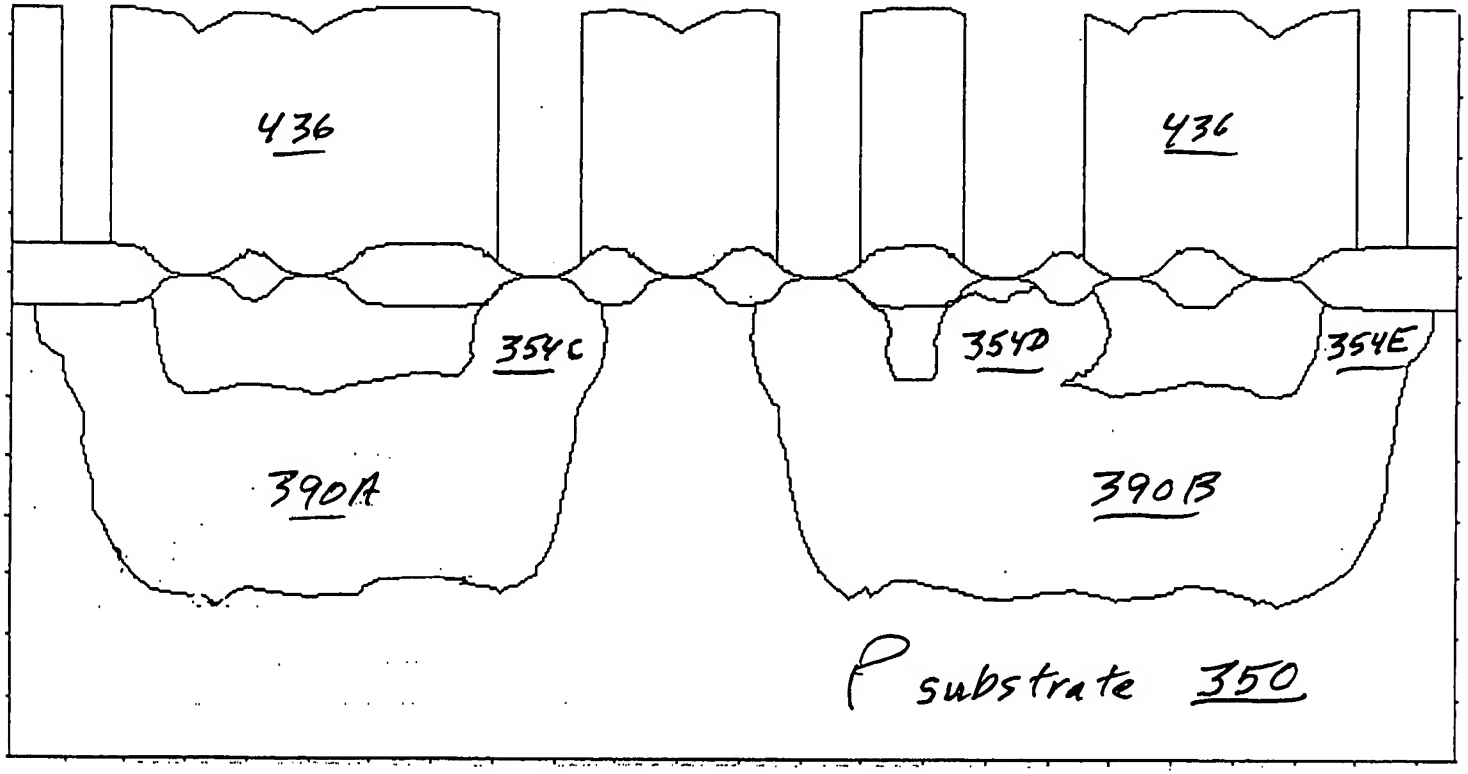
5V N Well Implant - First Stage

Fig. 40A

High F_T Layout

5V NPN 305

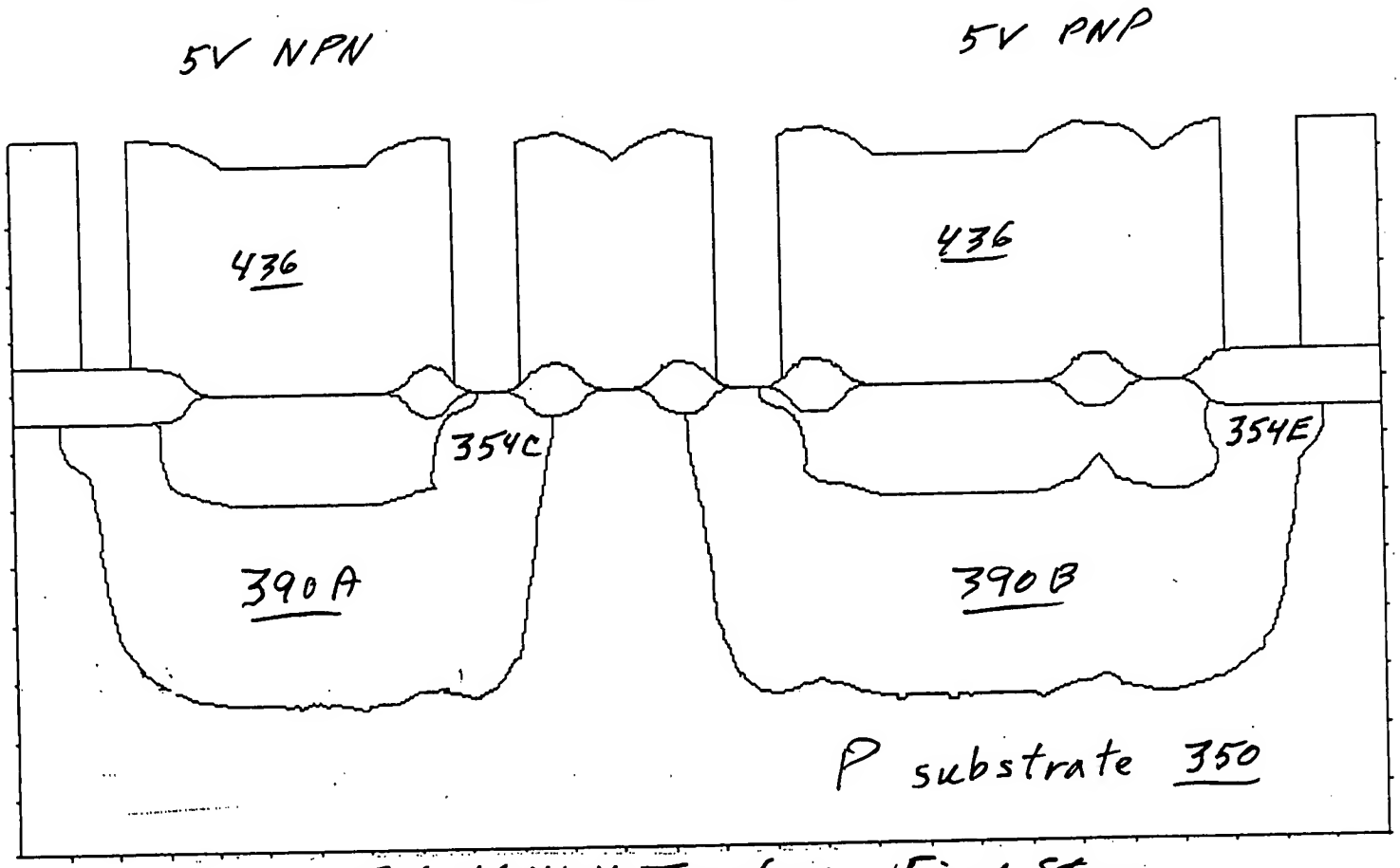
5V PNP 306



5V N Well Implant - First Stage

Fig. 40B

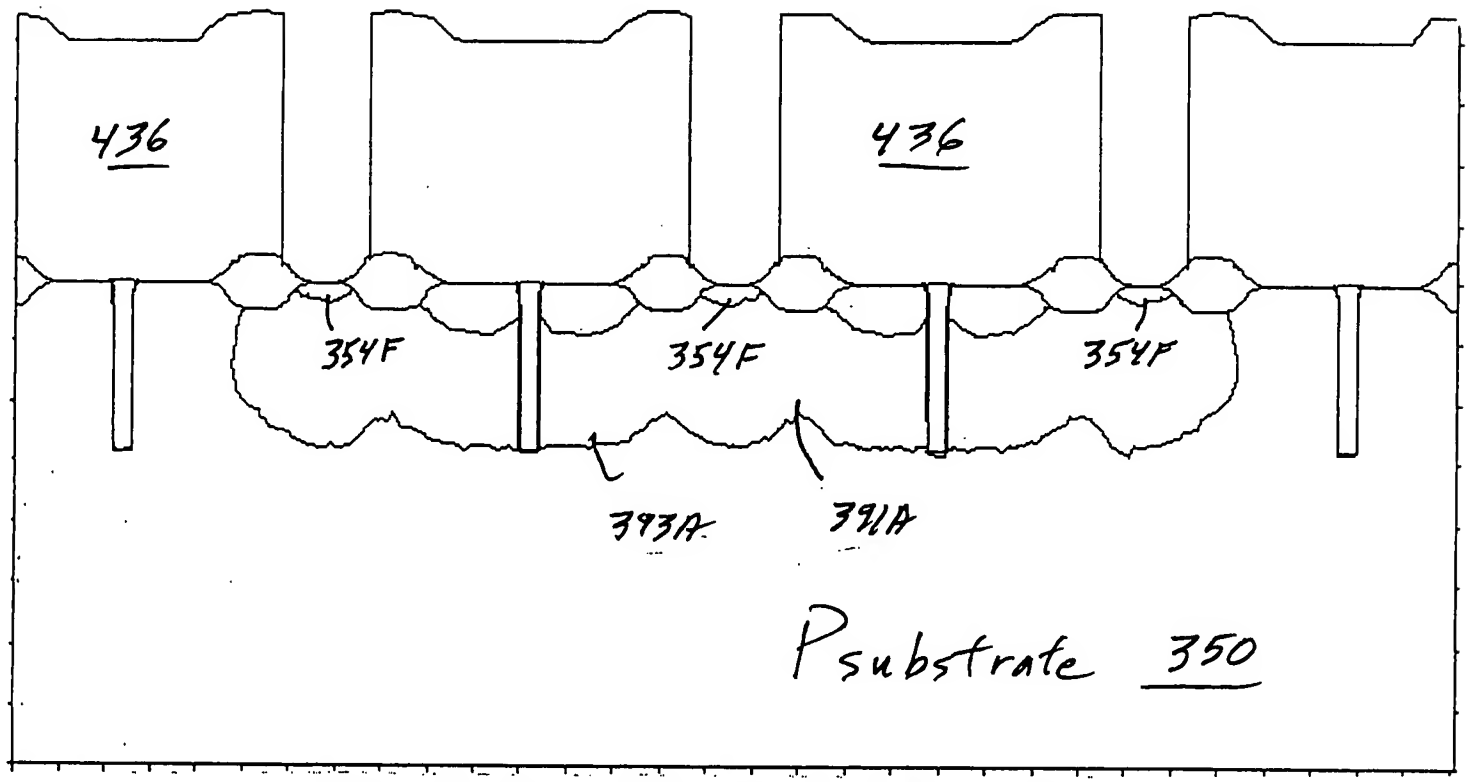
Conventional Layout



5V N Well Implant - First Stage

Fig. 40C

30V Lateral Trench DMOS 308

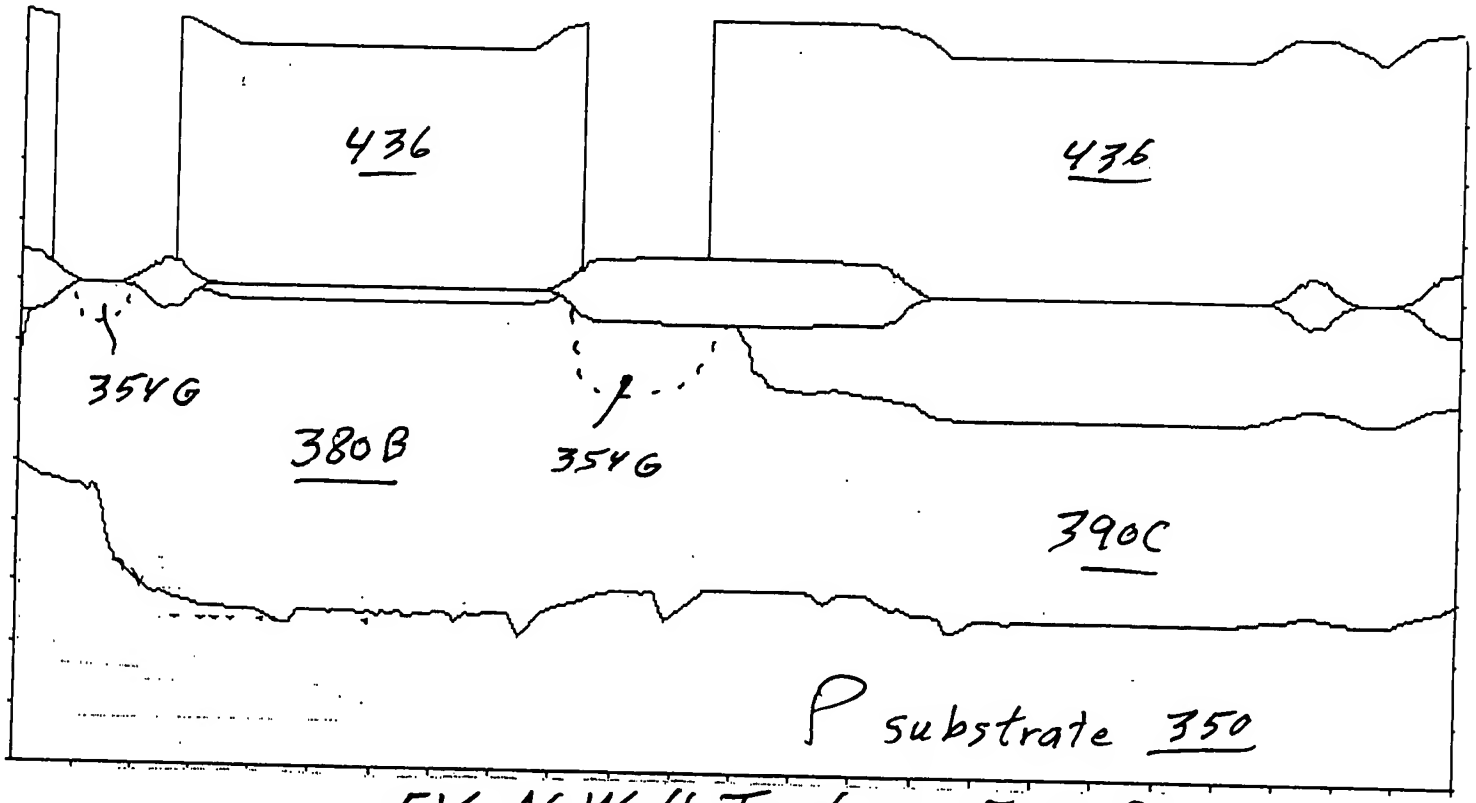


5V N Well Implant - First Stage

Fig 40D

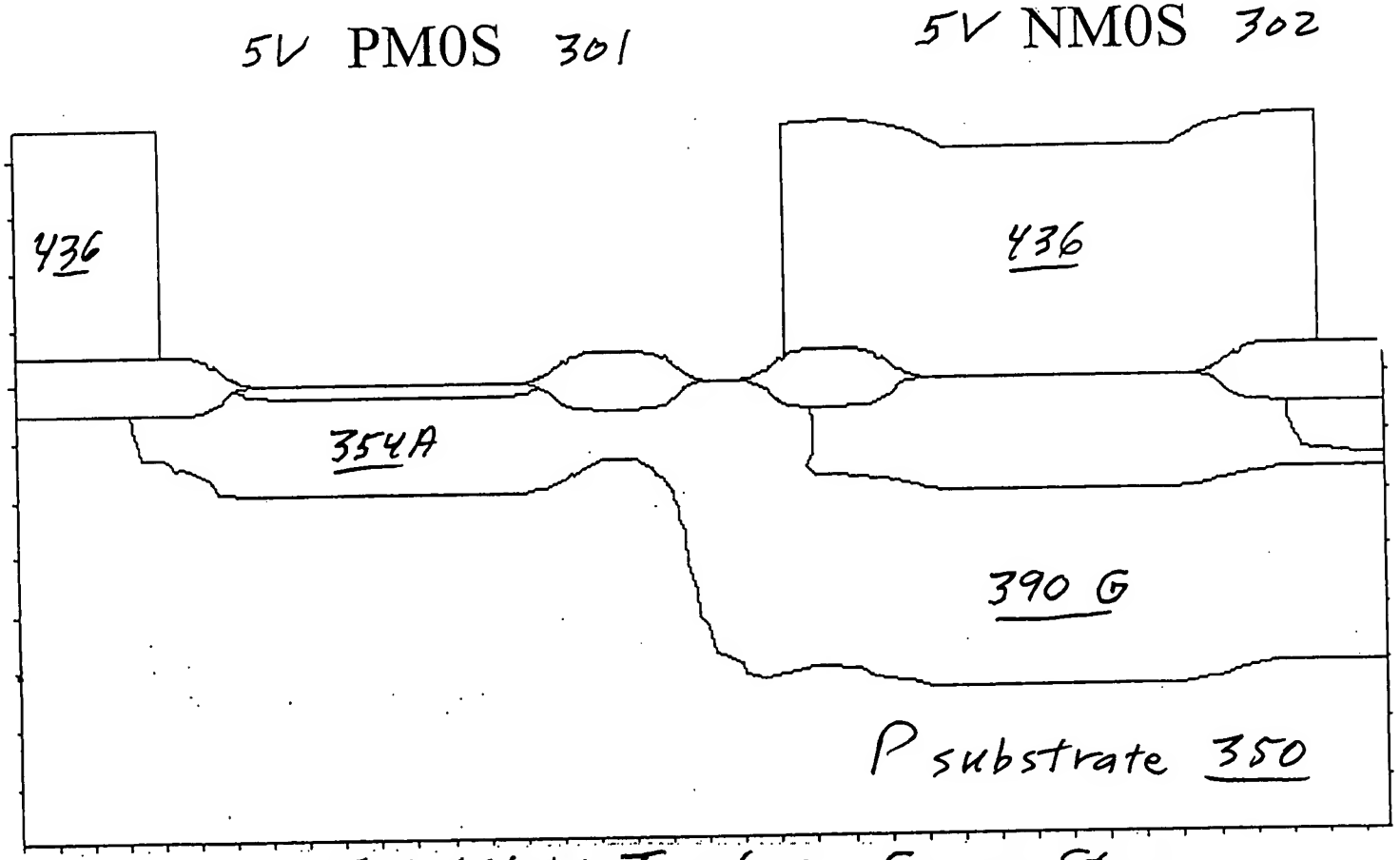
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



5V N Well Implant – First Stage

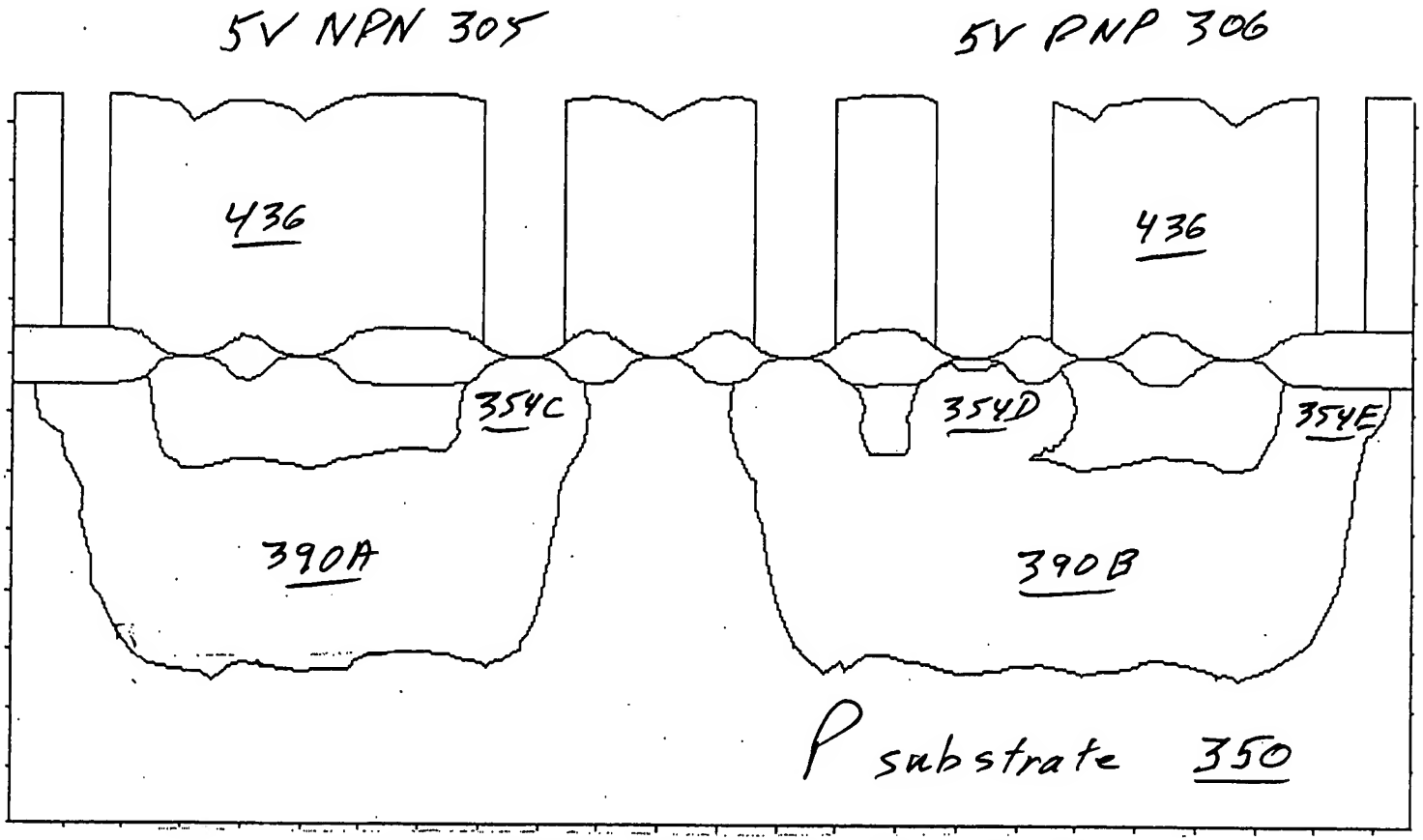
Fig 40E



5V N Well Implant - Second Stage

Fig. 41A

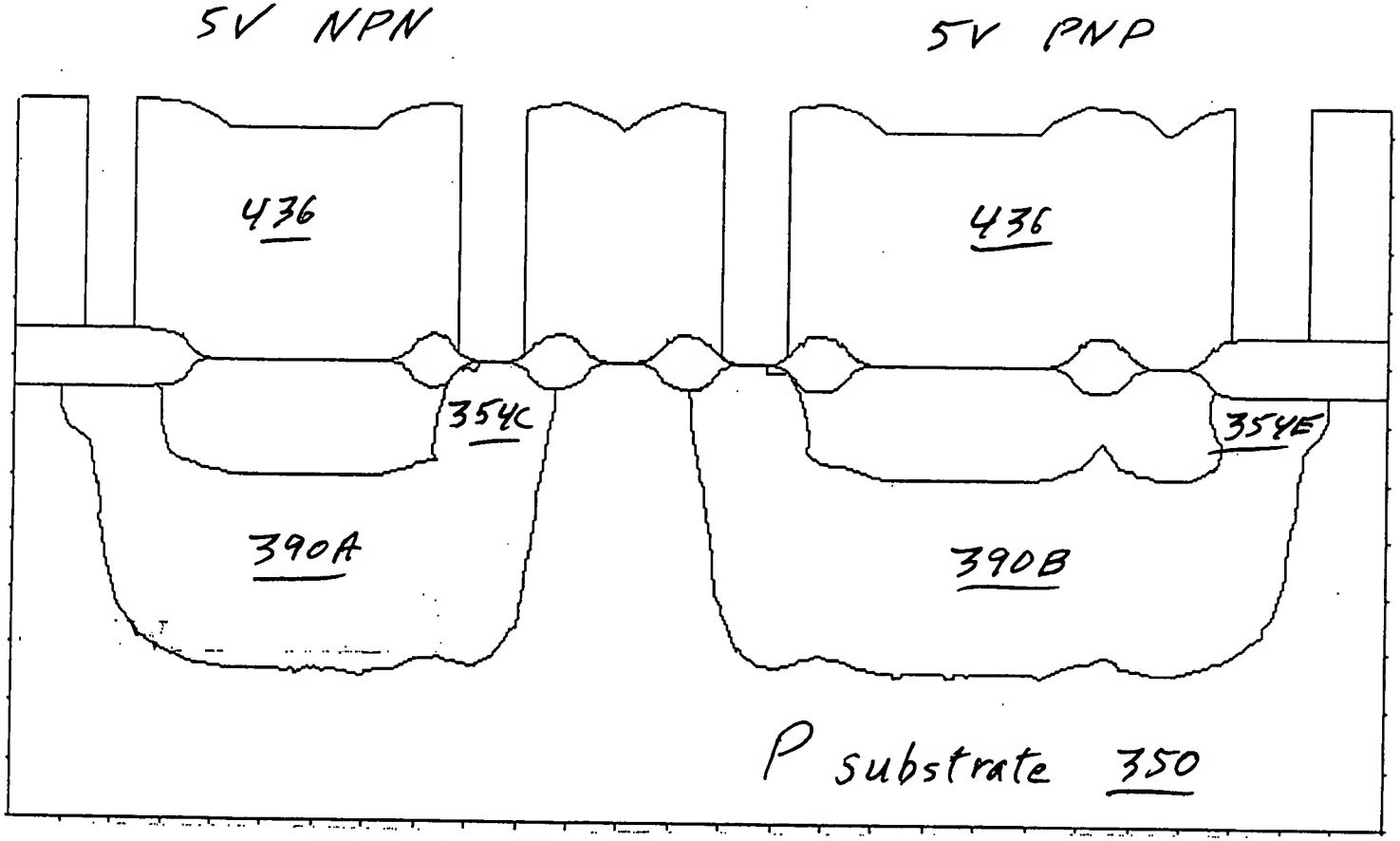
High F_T Layout



5V N Well Implant - Second Stage

Fig. 41B

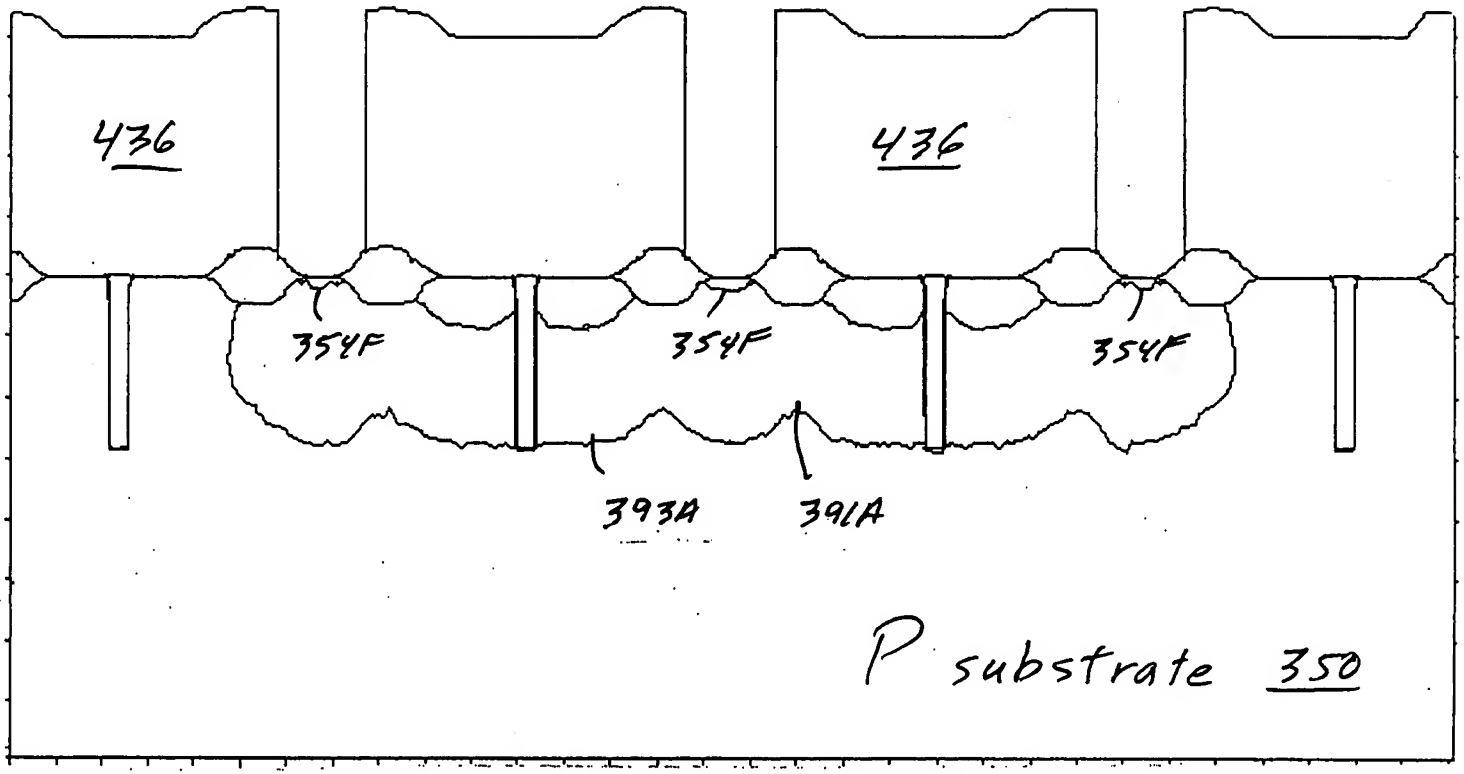
Conventional Layout



5V N Well Implant - Second Stage

Fig. 41C

30V Lateral Trench DMOS 308

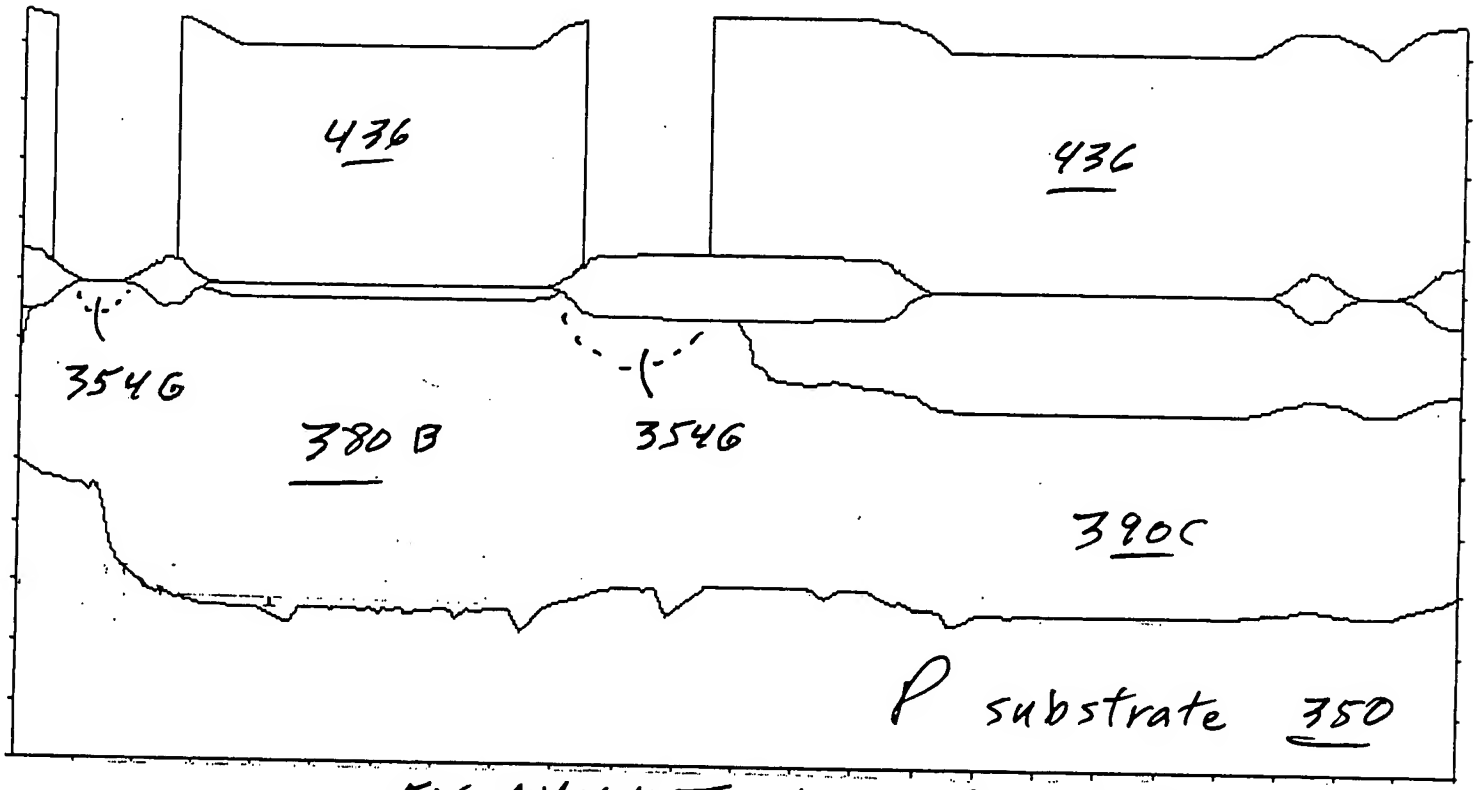


5V N Well Implant - Second Stage

Fig. 41D

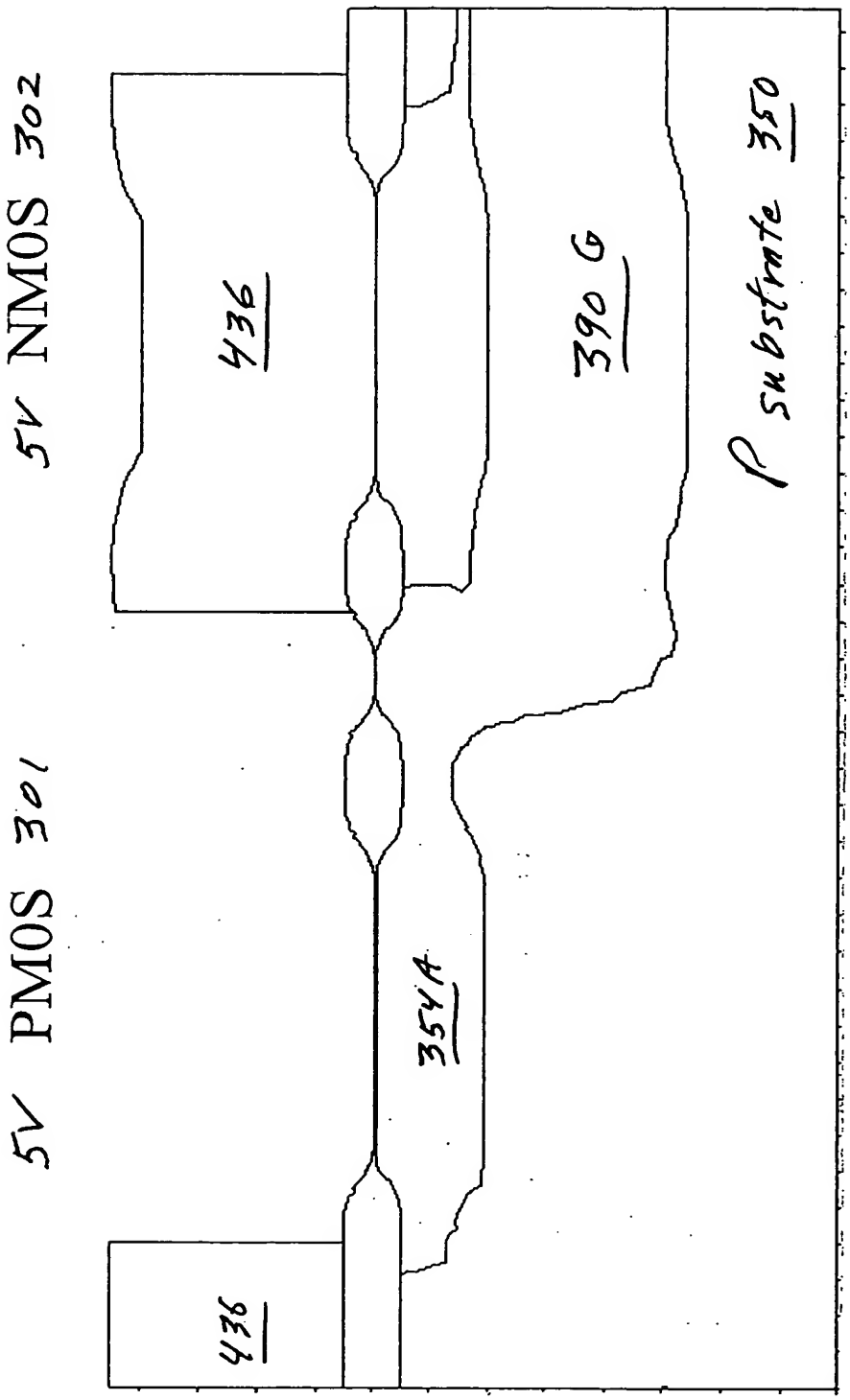
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



5V NWell Implant - Second Stage

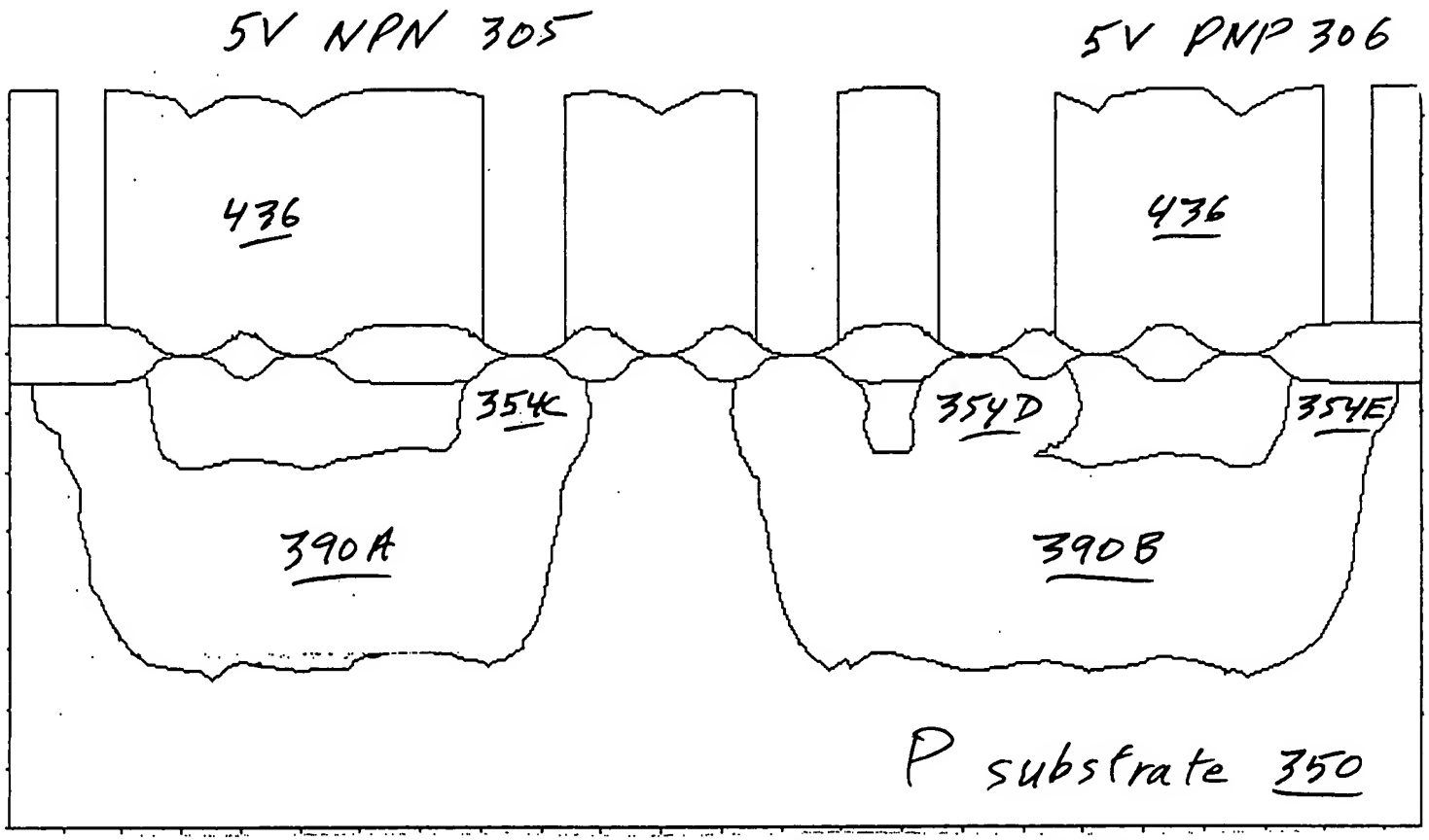
Fig. 41E



5V N Well Implant - Third Stage

Fig. 42A

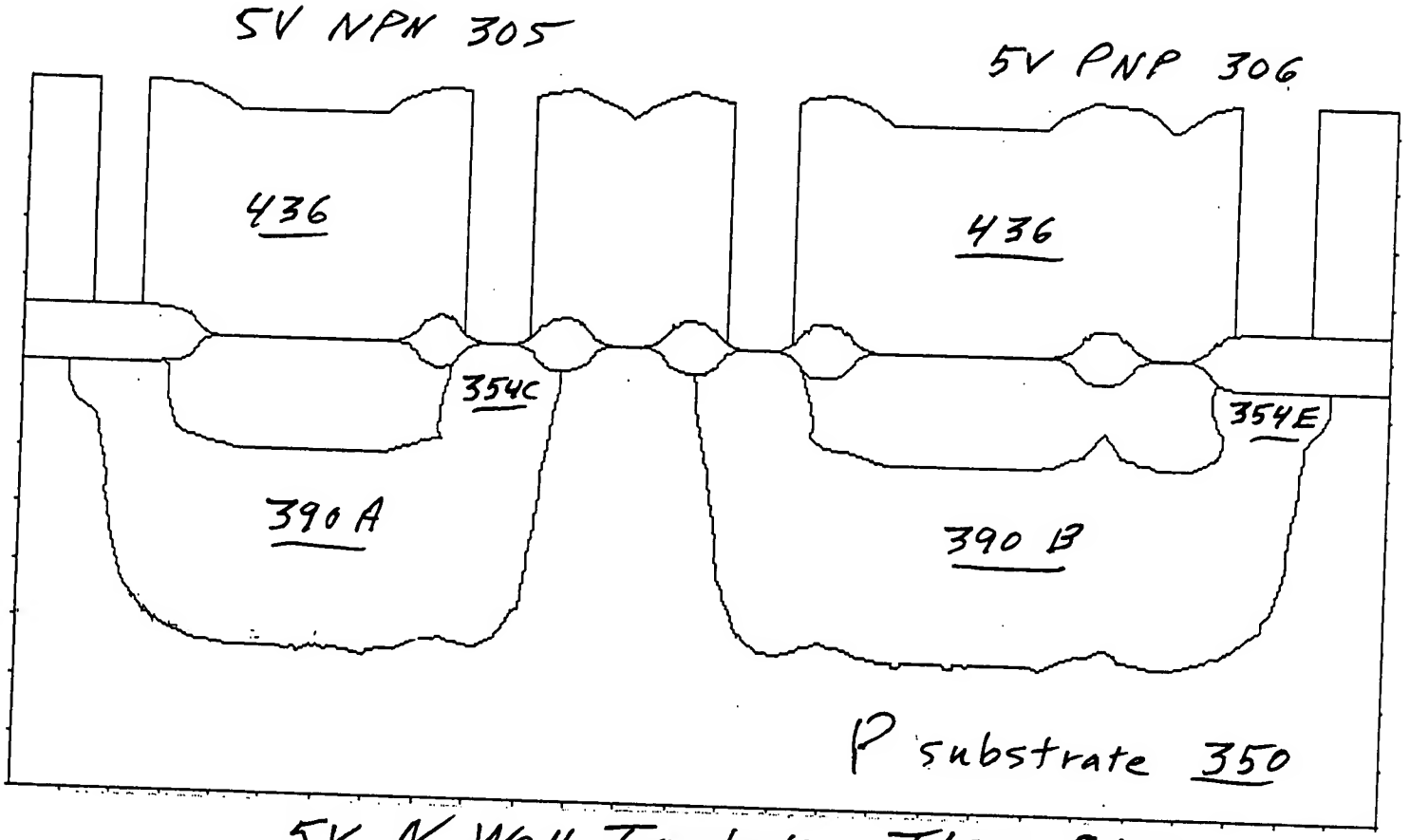
High F_T Layout



5V N Well Implant - Third Stage

Fig. 42B

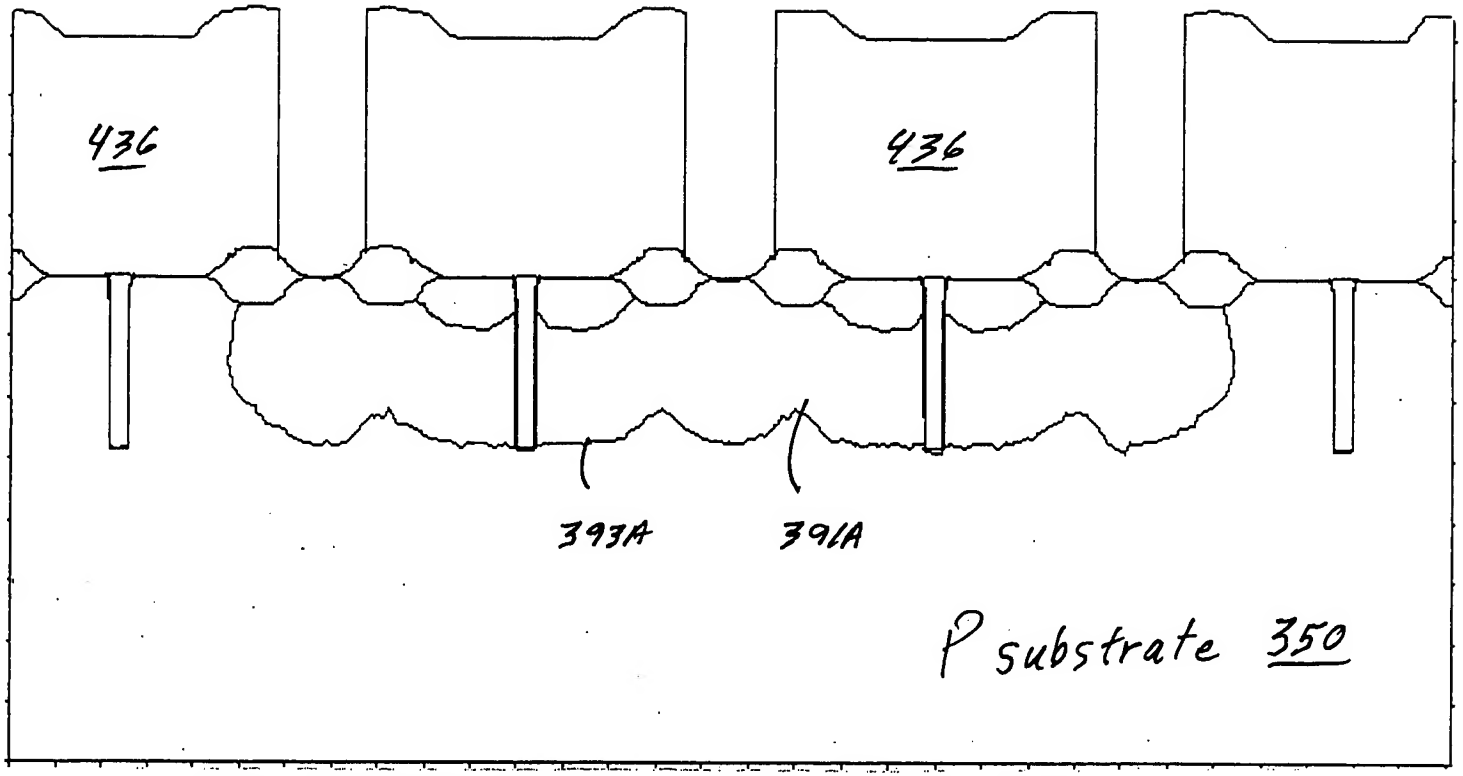
Conventional Layout



5V N Well Implant – Third Stage

Fig. 42C

30V Lateral Trench DMOS 308

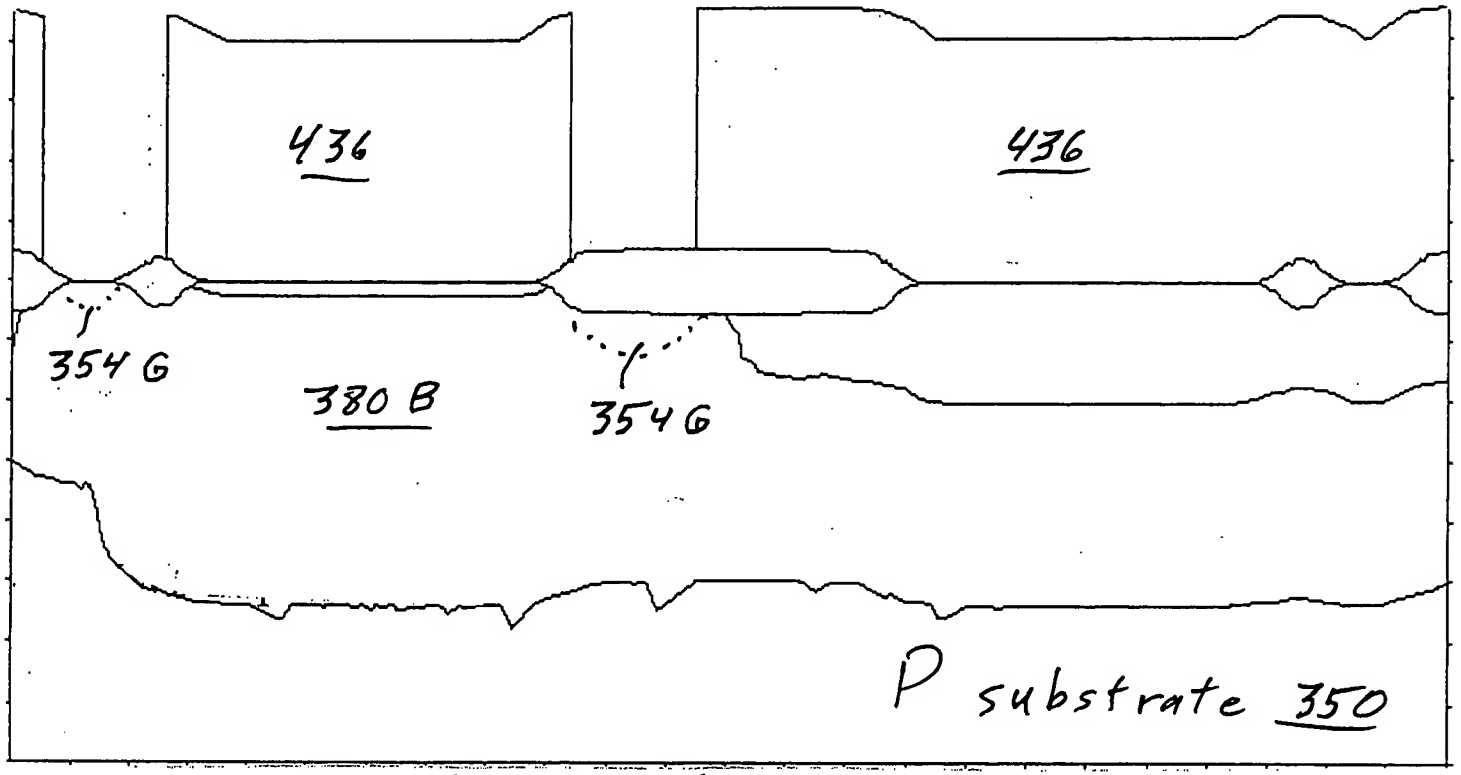


5V N Well Implant - Third Stage

Fig. 42D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



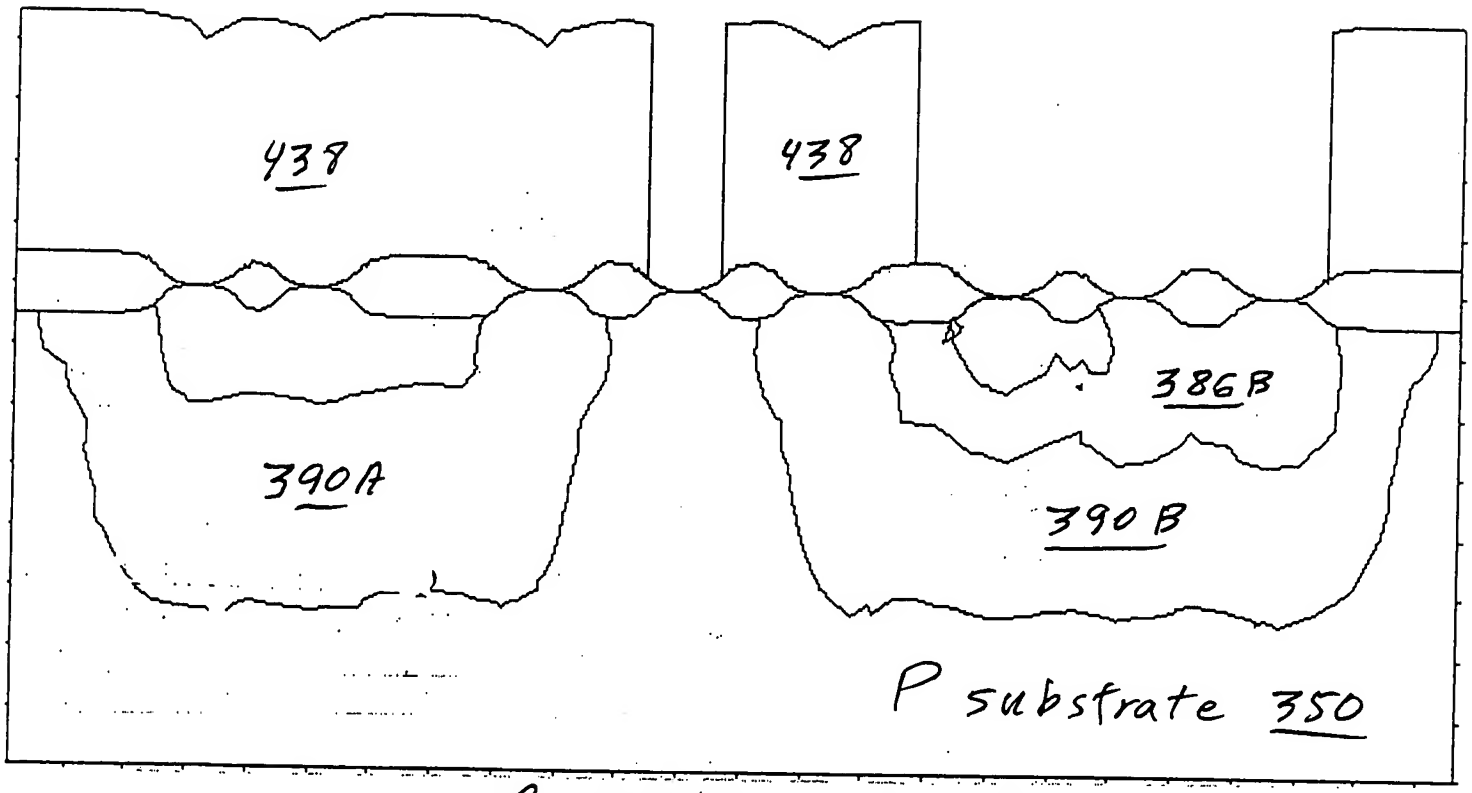
5V N Well Implant – Third Stage

Fig. 42E

High F_T Layout

5V NPN 305

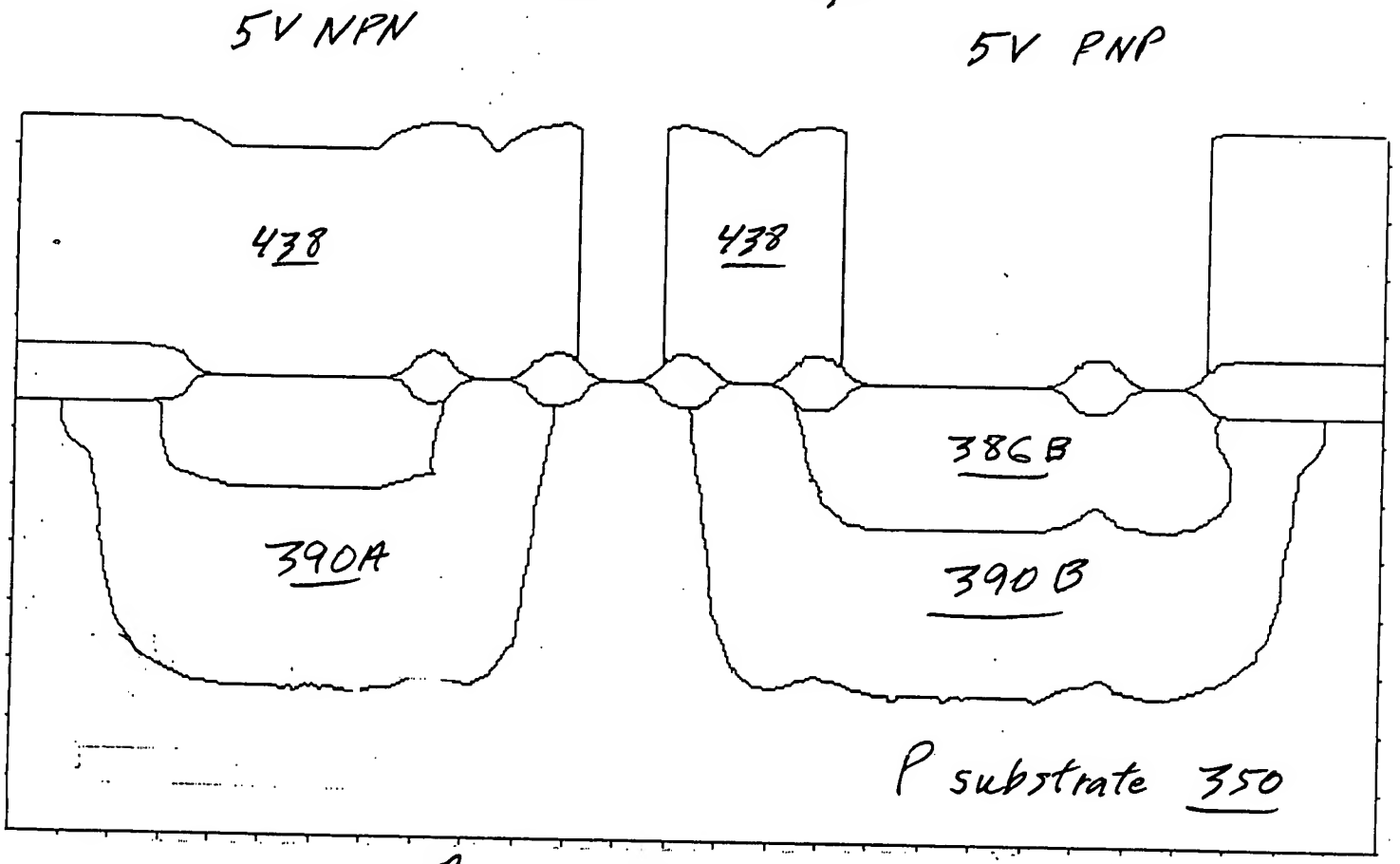
5V PNP 306



12V P Well Implant - First Stage

Fig. 43B

Conventional Layout

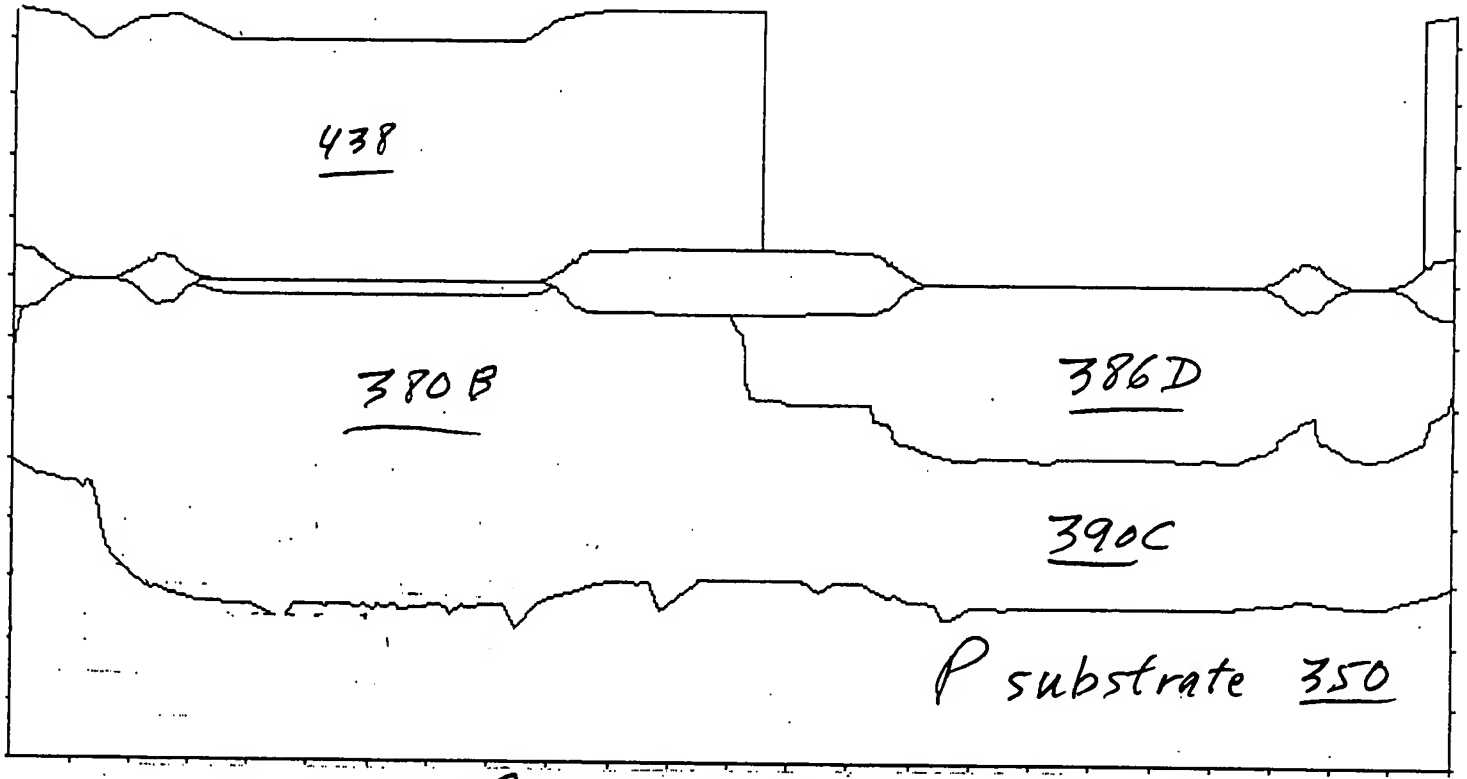


12V P Well Implant - First Stage

Fig. 43C

Symmetrical 12V CMOS

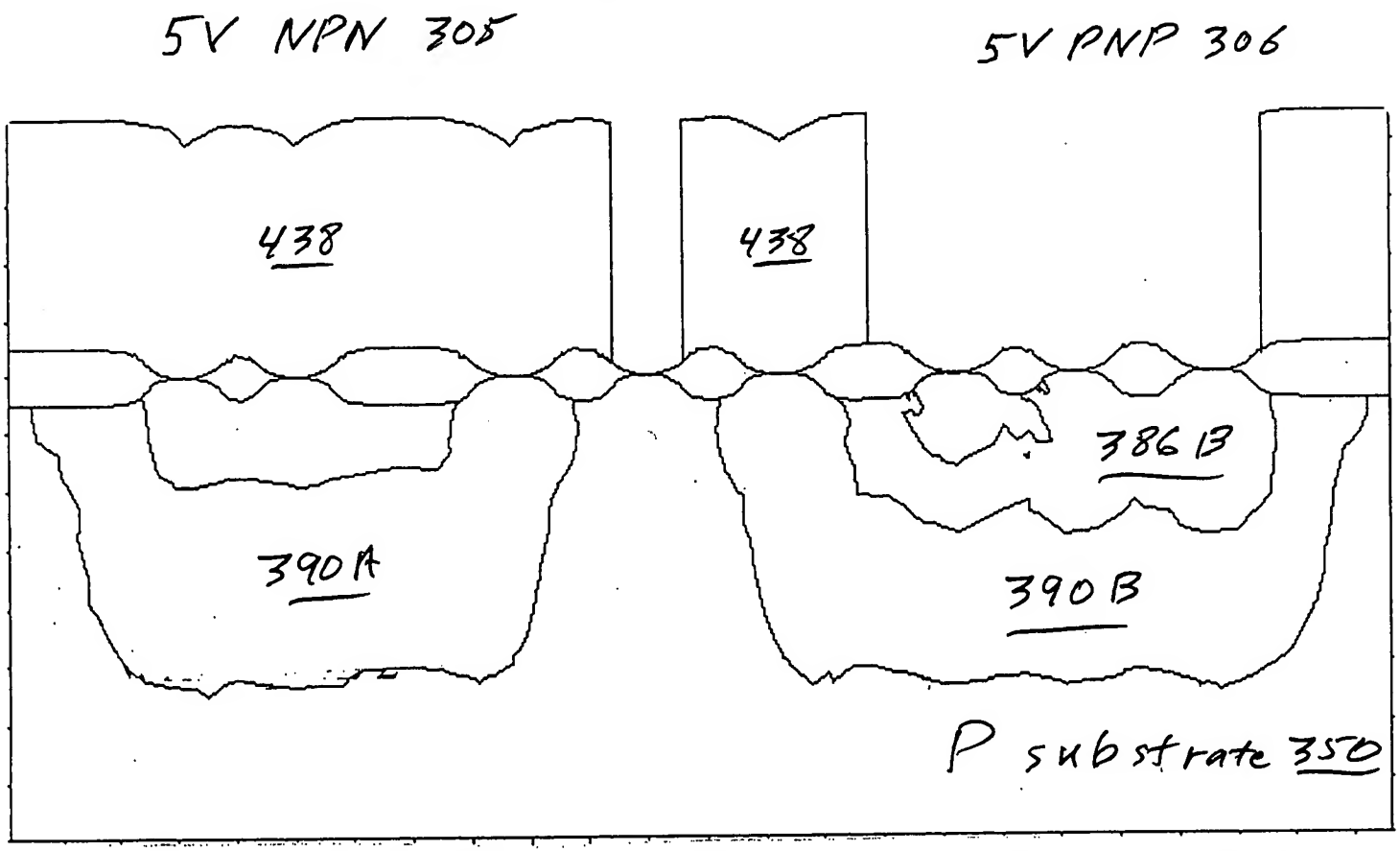
12V PMOS 309 12V NMOS 310



12V PWell Implant - First Stage

Fig 43E

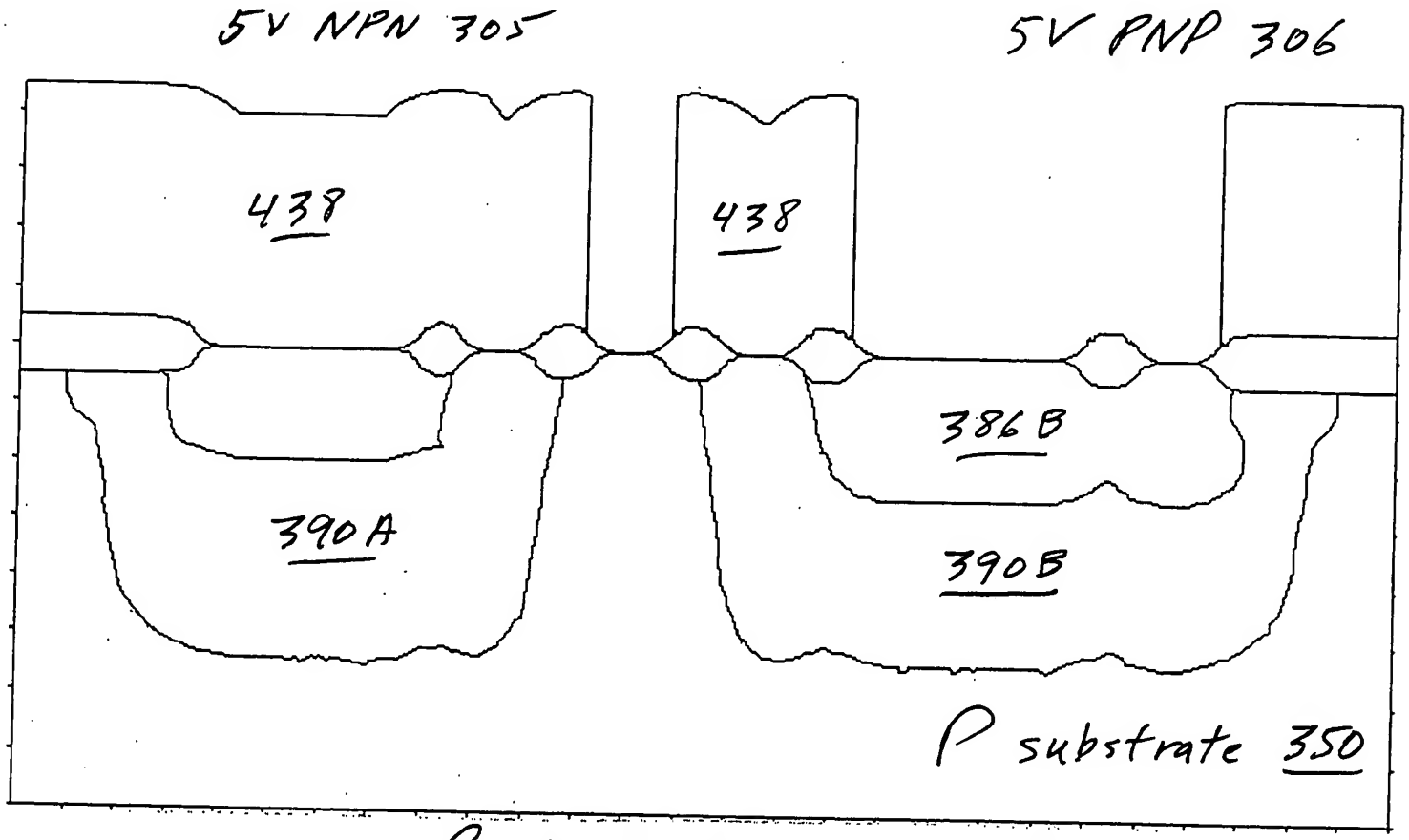
High F_T Layout



12V P Well Implant - Second Stage

Fig. 44B

Conventional Layout

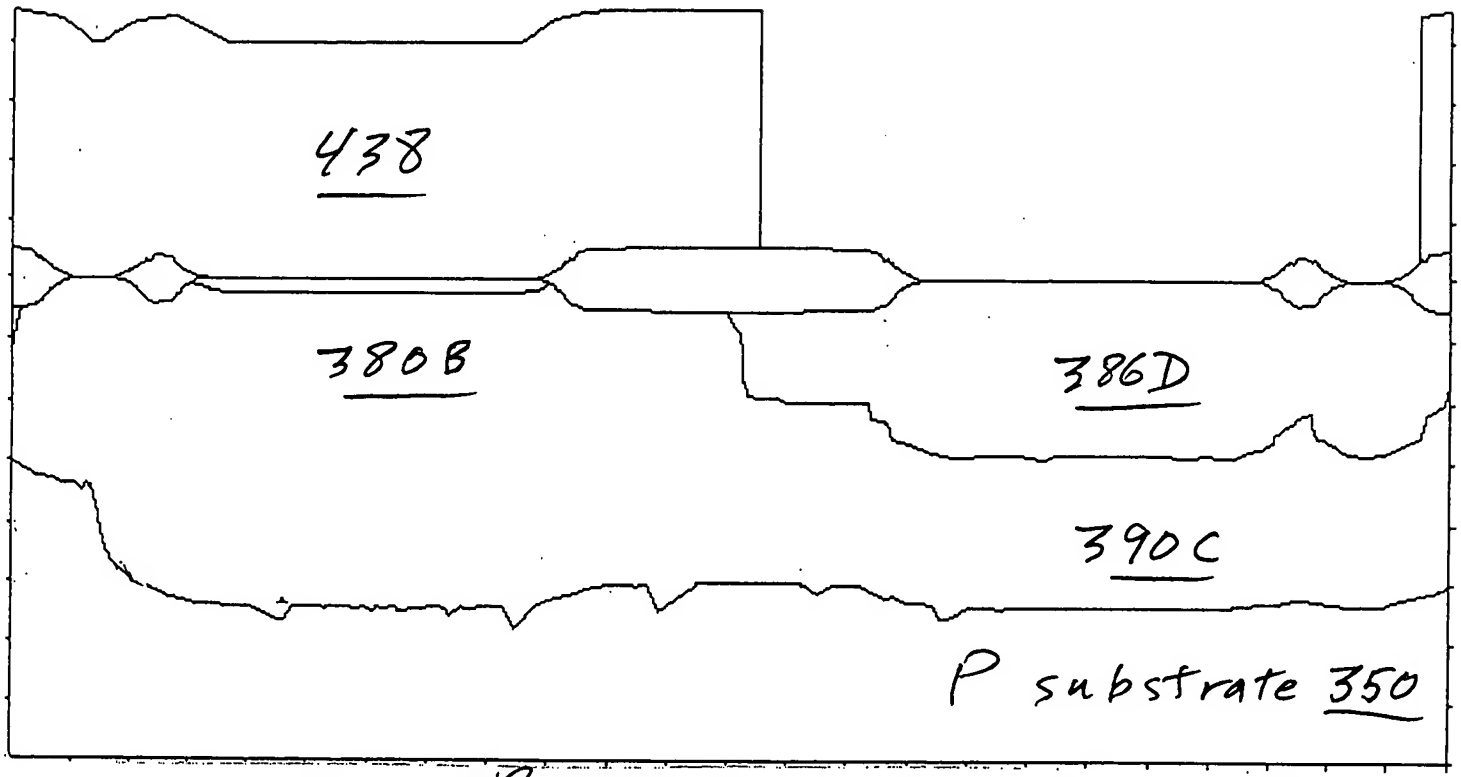


12V P Well Implant - Second Stage

Fig 44C

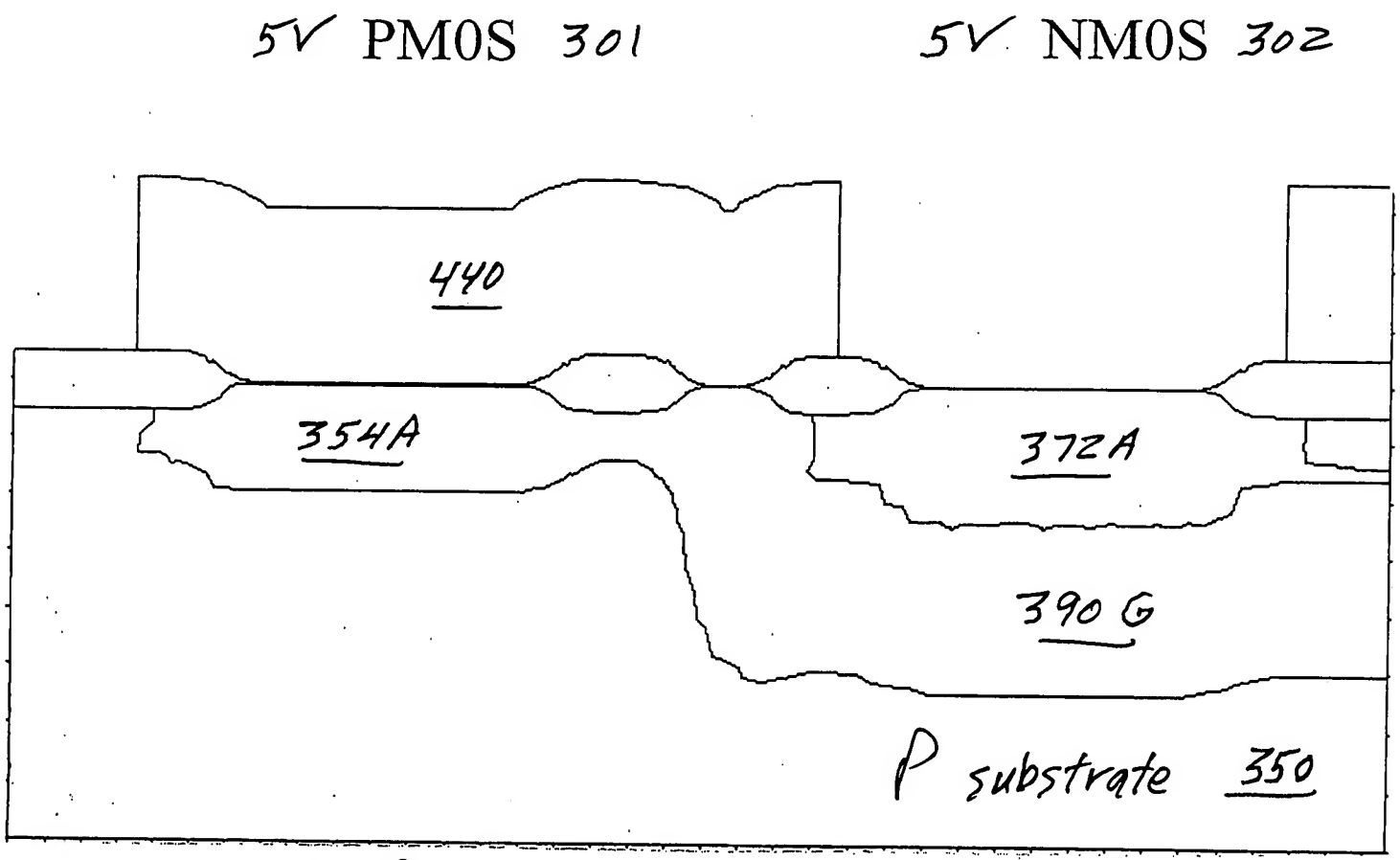
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



12 V P Well Implant – Second Stage

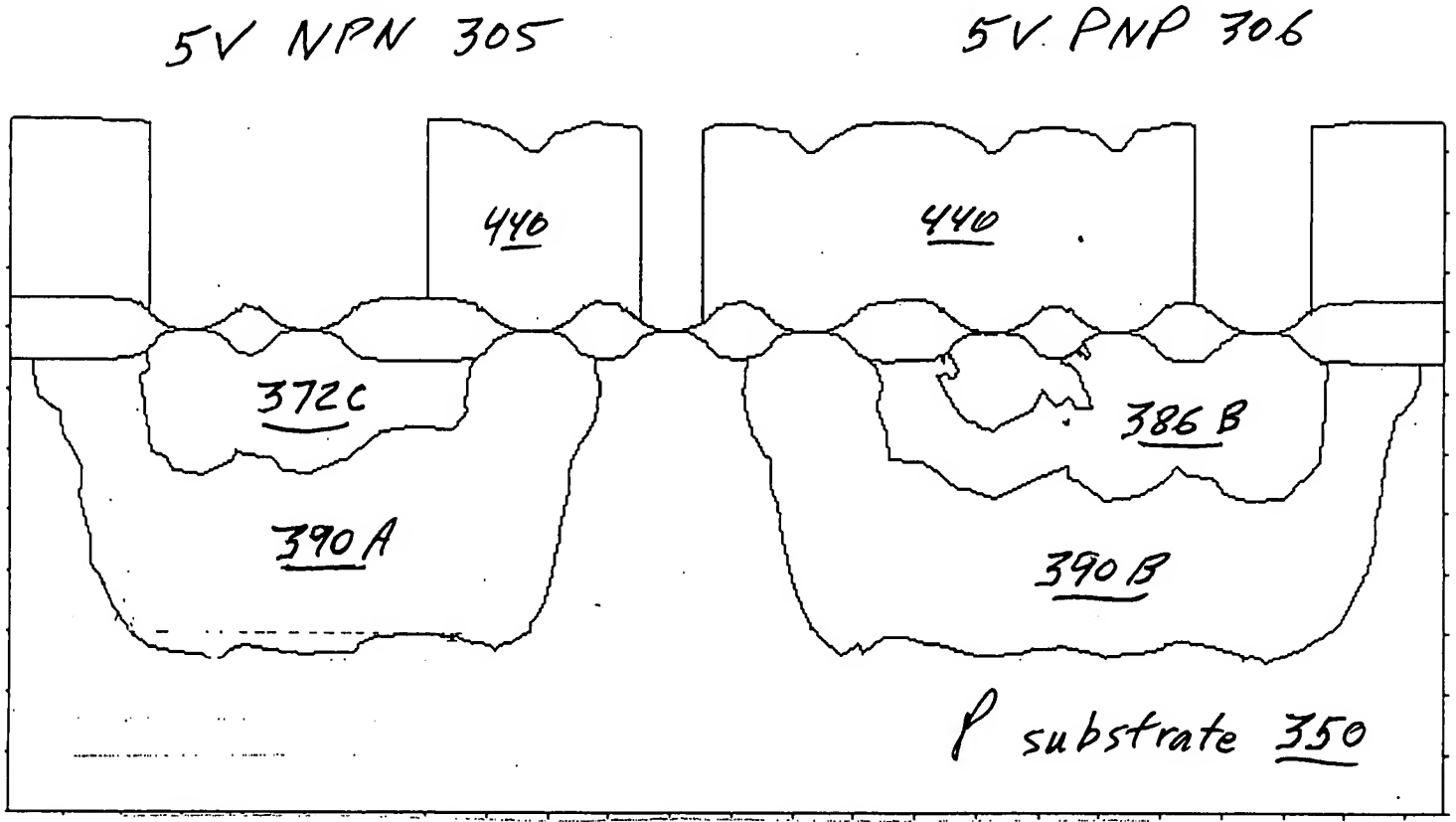
Fig. 44E



5 V P Well Implant - First Stage

Fig. 45A

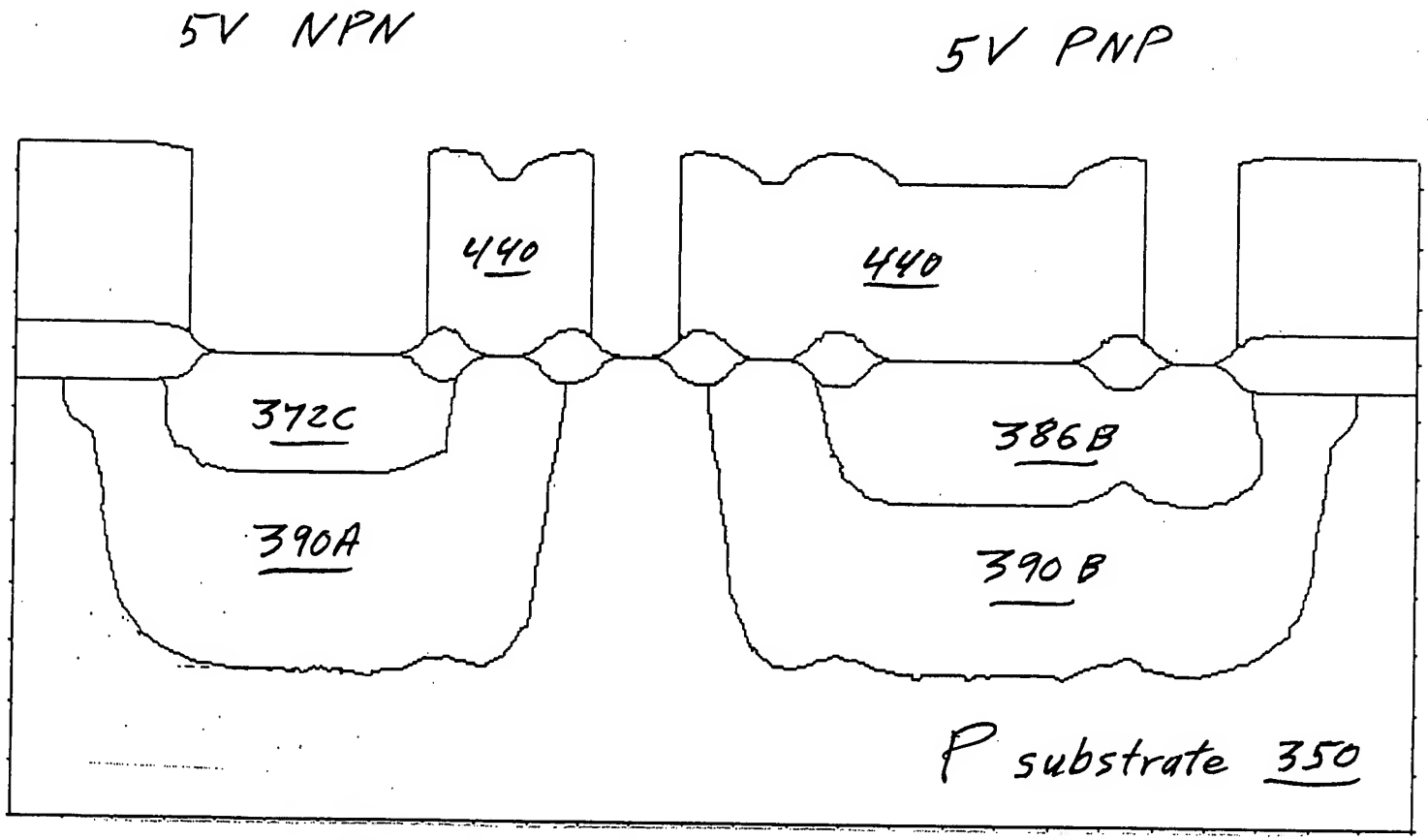
High F_T Layout



5V P Well Implant – First Stage

Fig. 45B

Conventional Layout

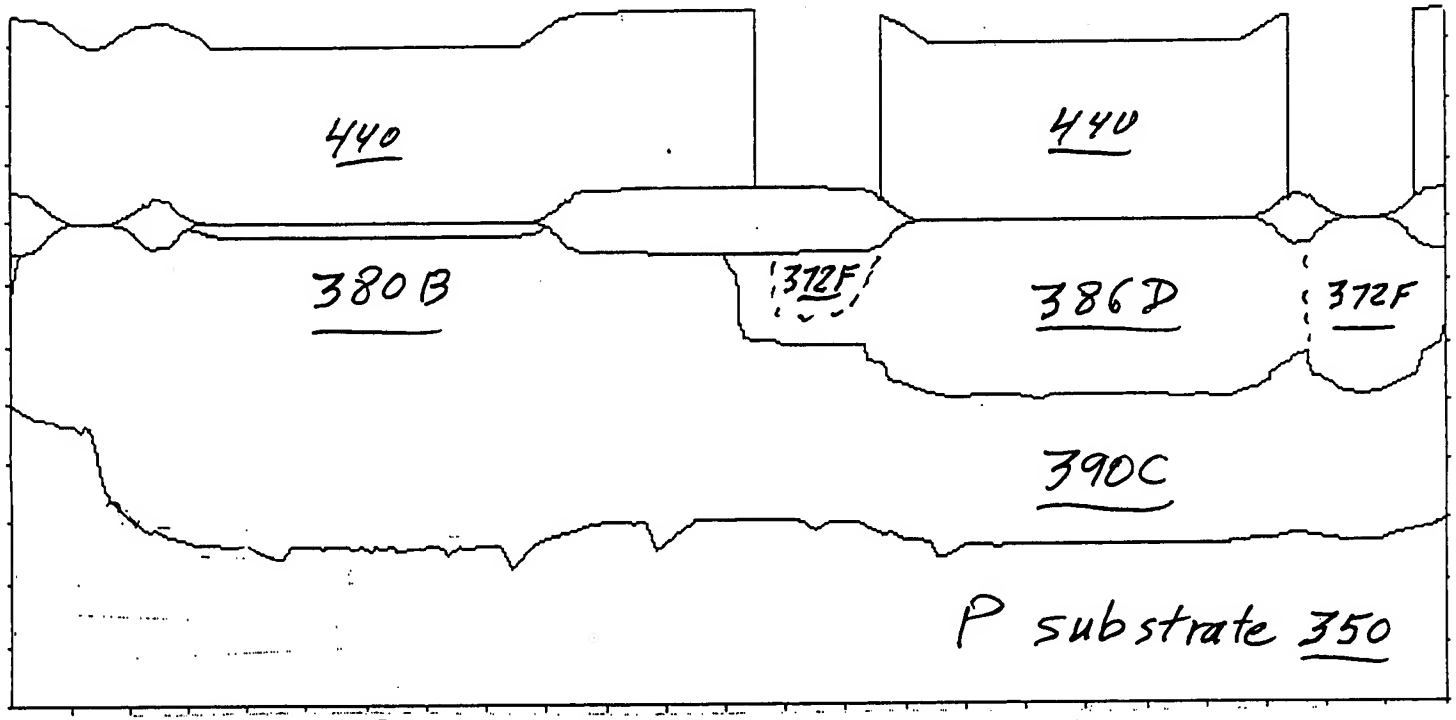


5V P Well Implant - First Stage

Fig. 45C

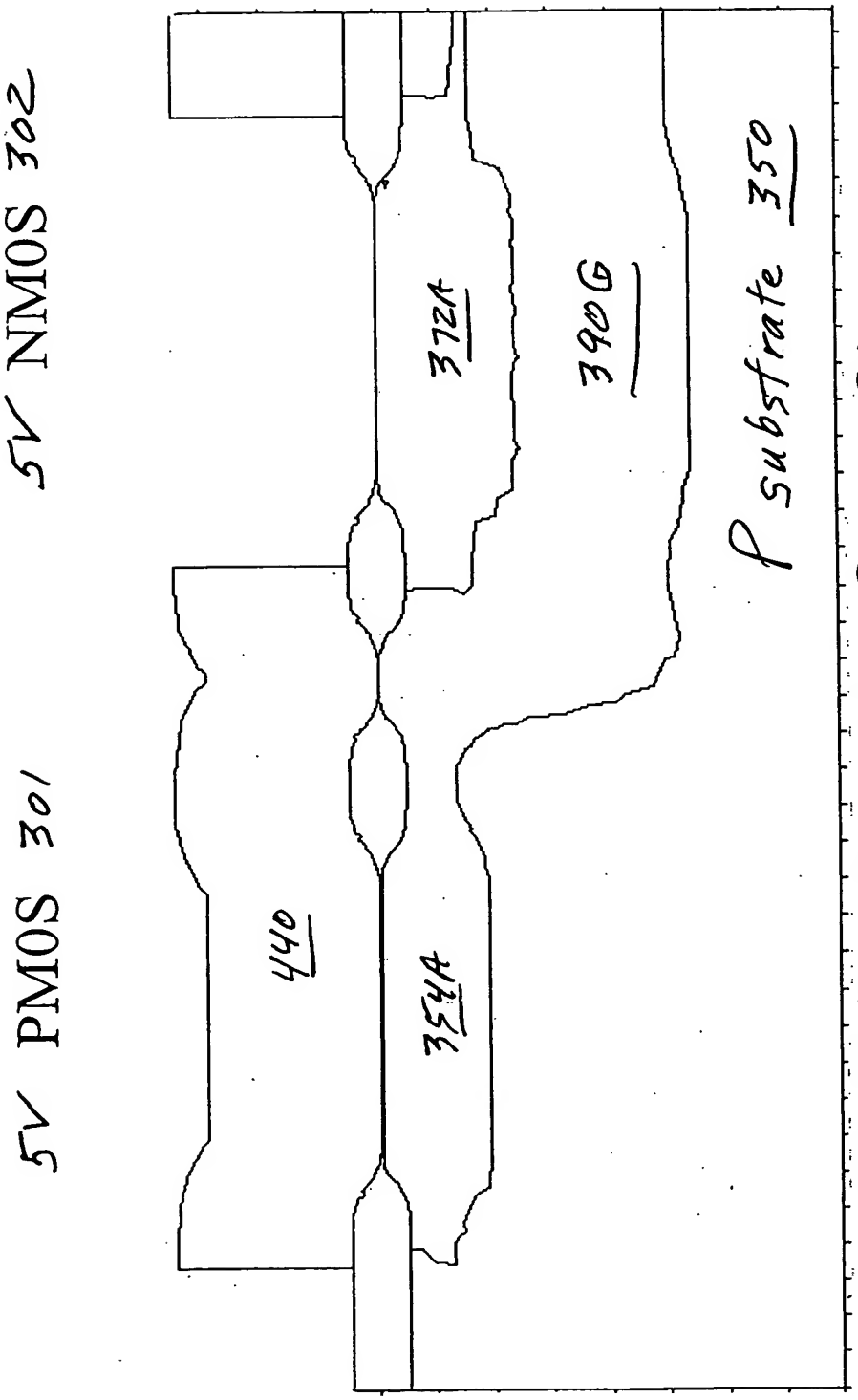
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



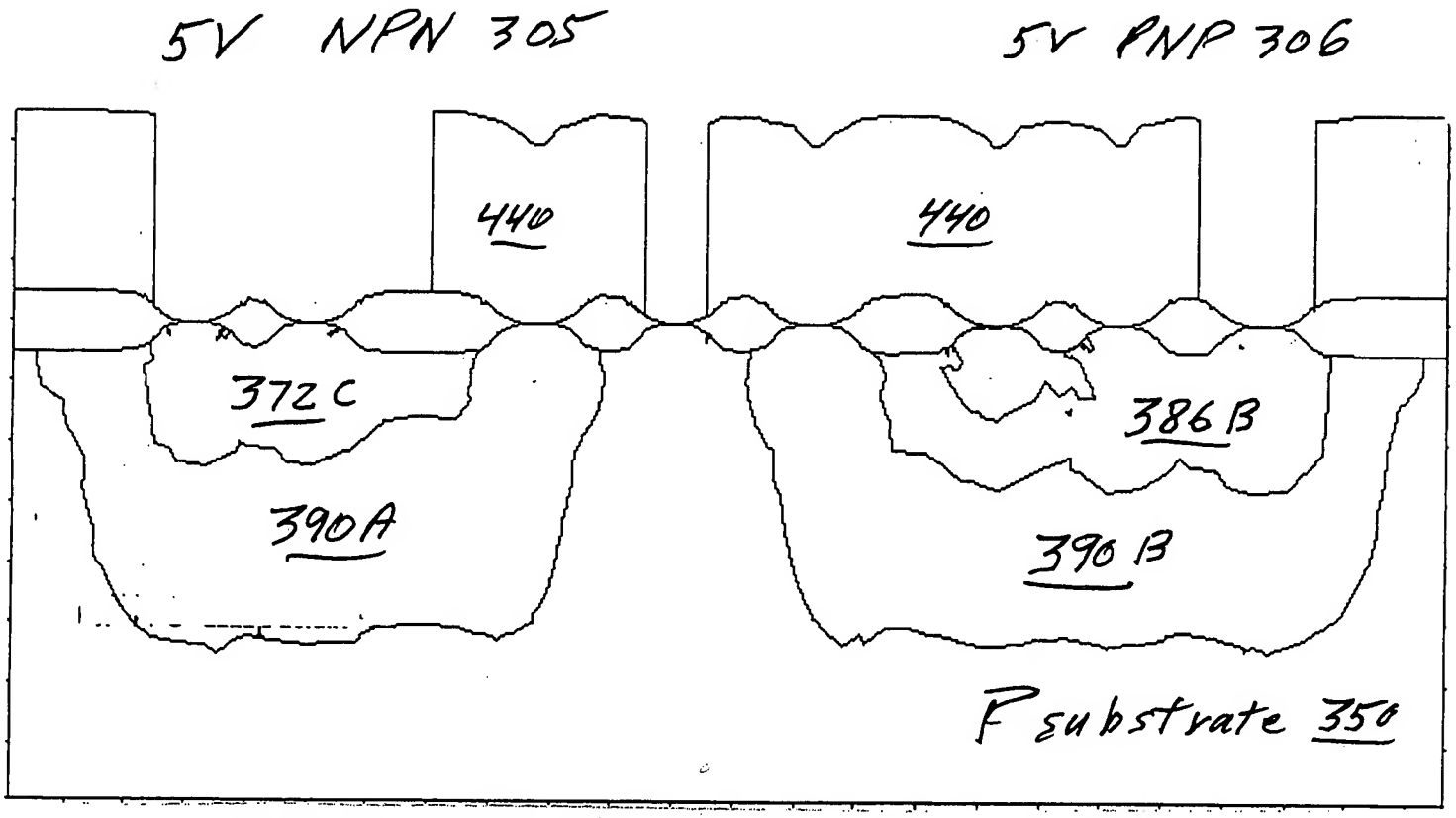
5V P Well Implant – First Stage

Fig. 45E



5V P Well Implant - Second Stage
Fig. 2 46A

High F_T Layout

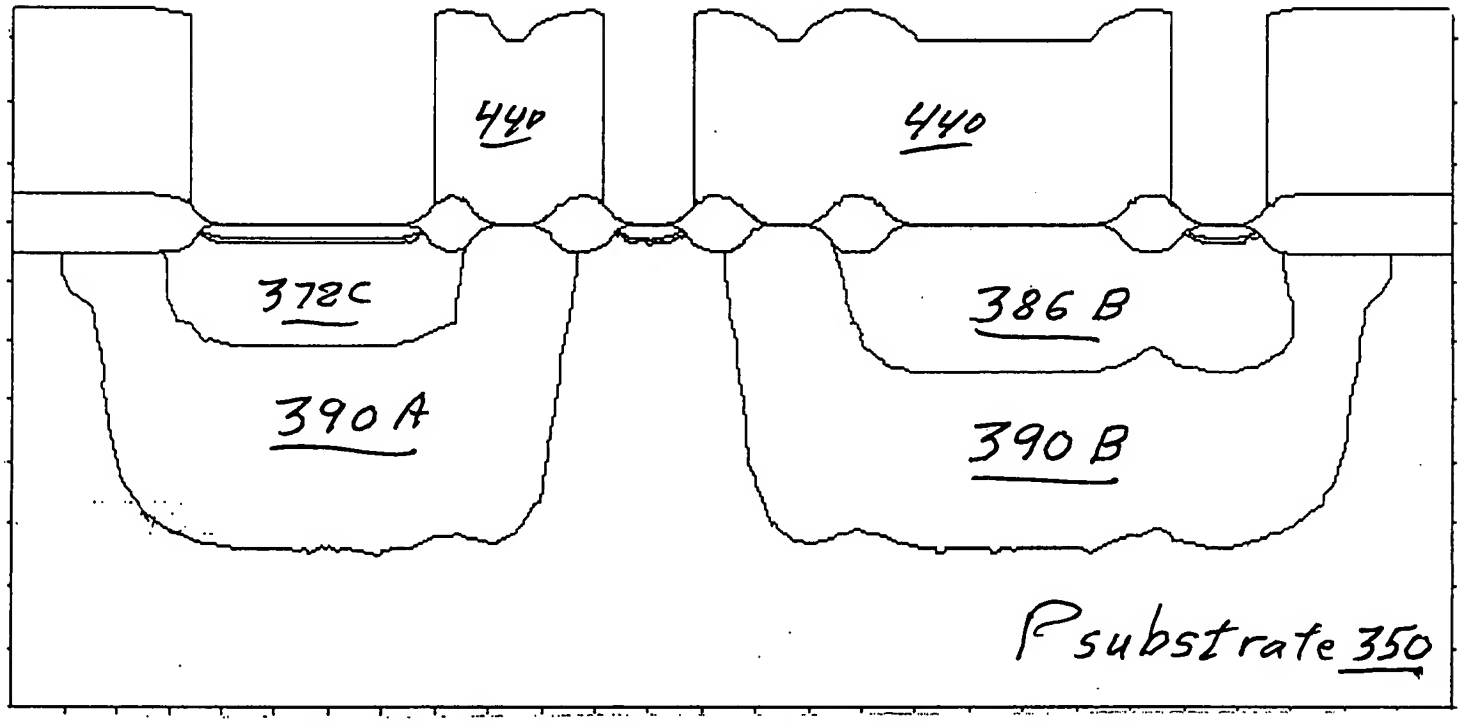


5V P Well Implant - Second Stage

Fig. 46B

Conventional Layout

5V NPN 305 5V PNP 306

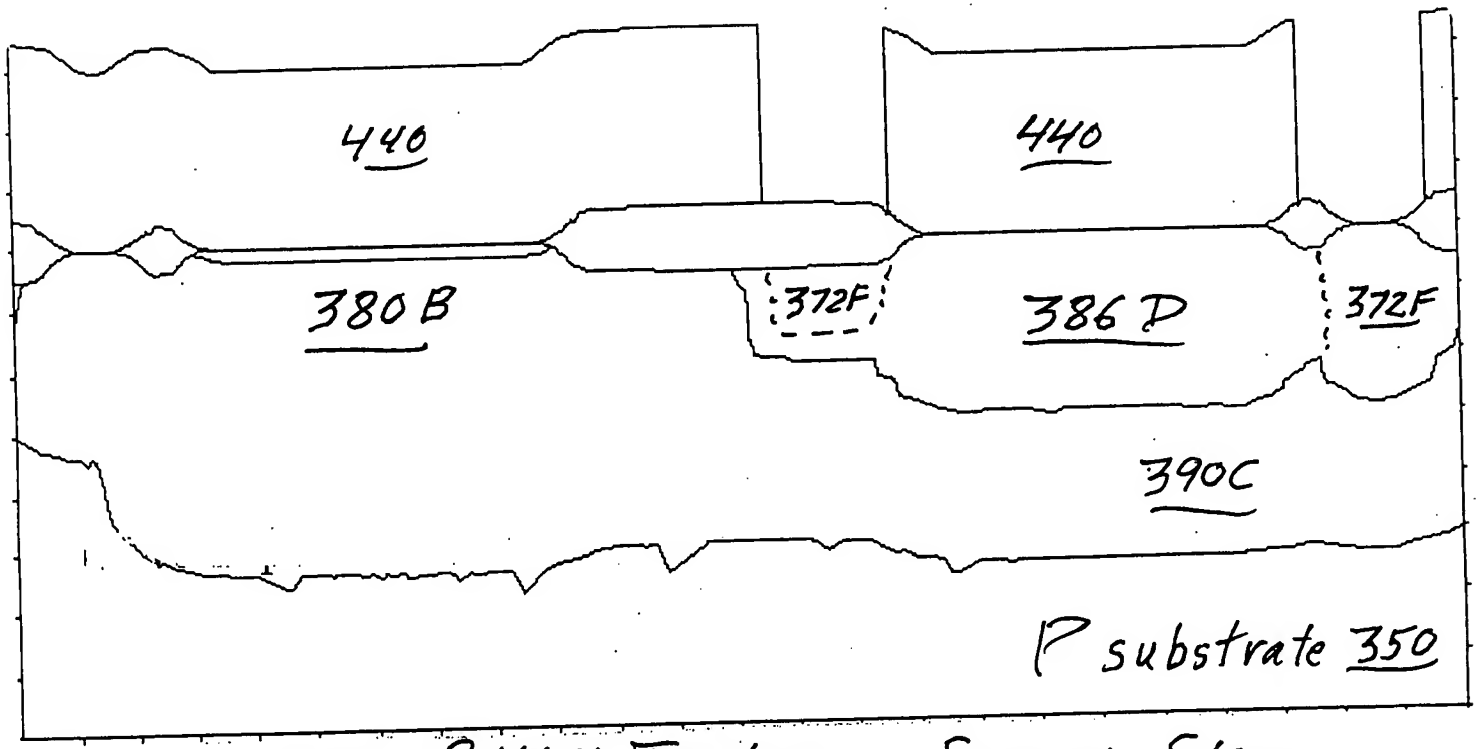


5V P Well Implant - Second Stage

Fig. 46C

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

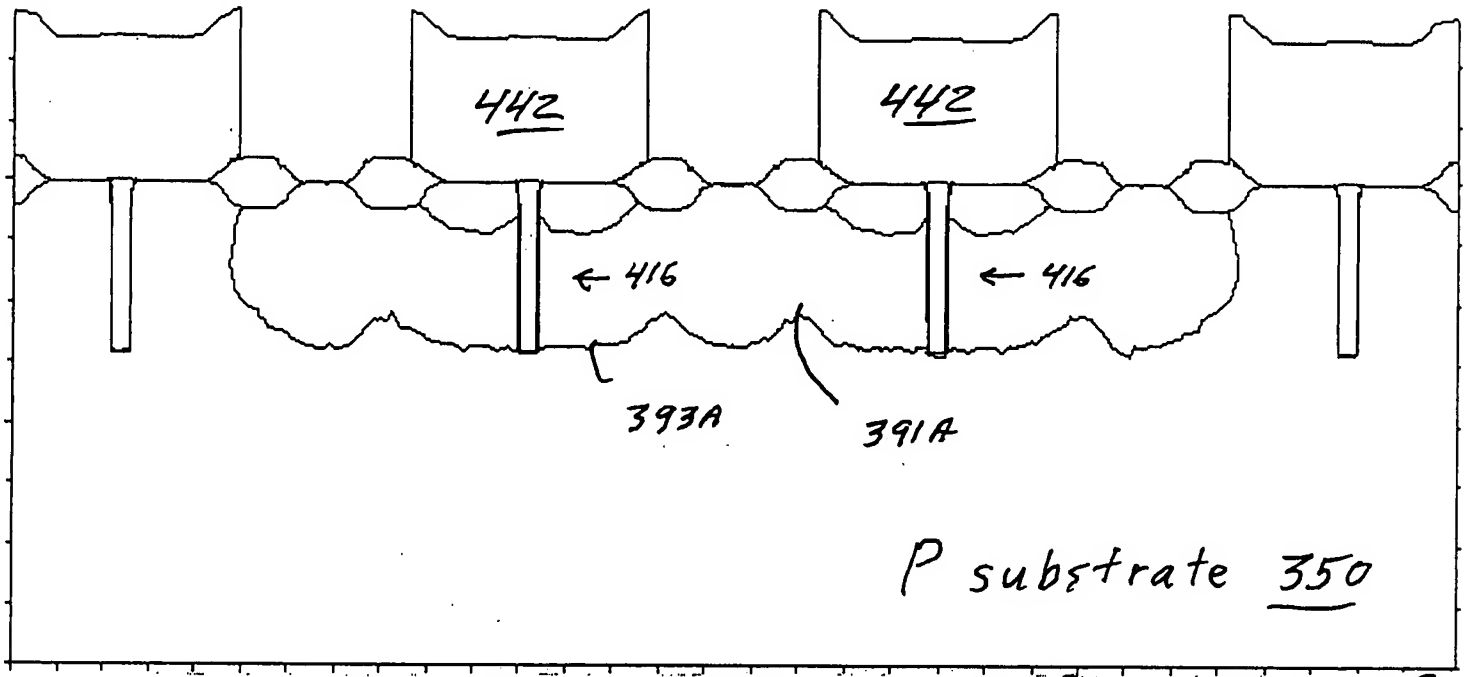


5V P Well Implant – Second Stage

Fig. 46E

612/641

30V Lateral Trench DMOS 308



Etch - Block Mask and Etching of Planar Active Regions

Fig. 47D

5V PMOS 301 5V NMOS 302

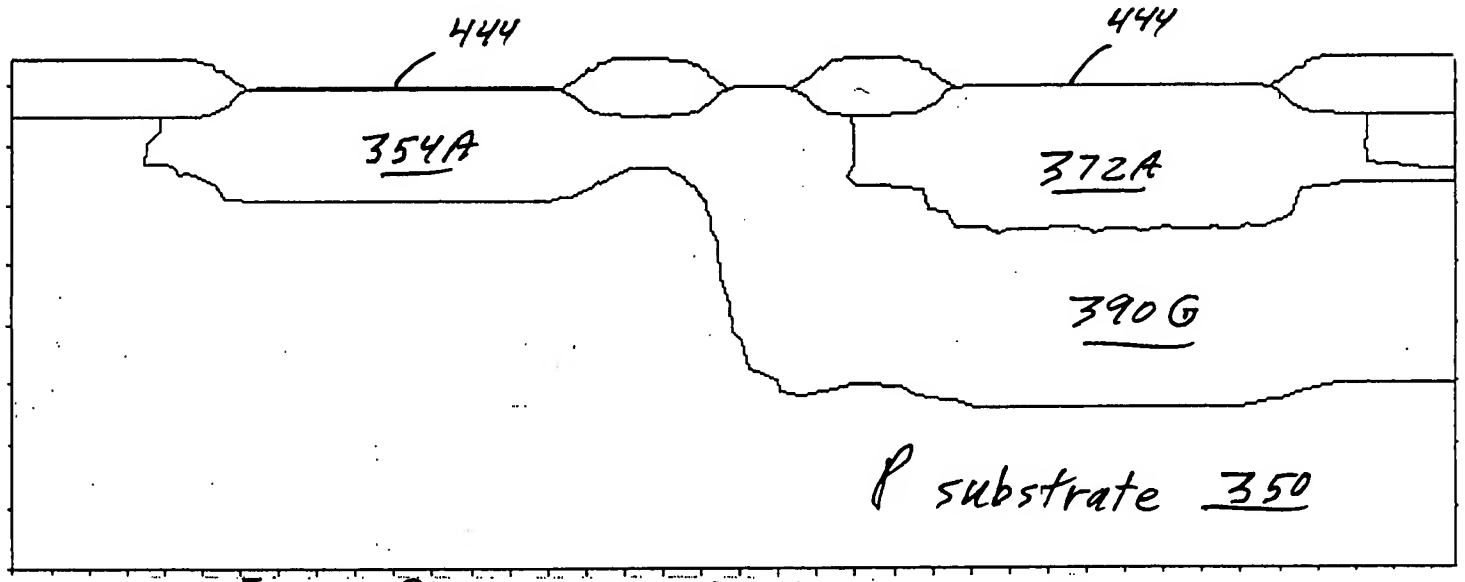
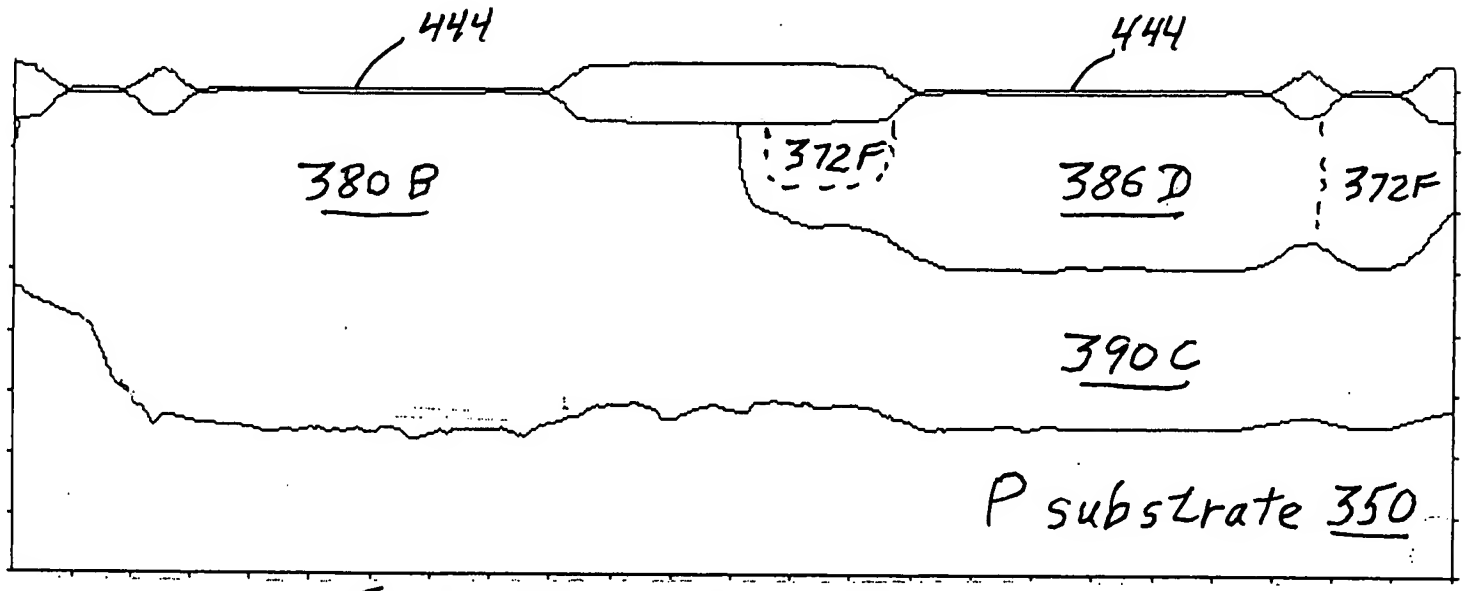


Fig. 4BA

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

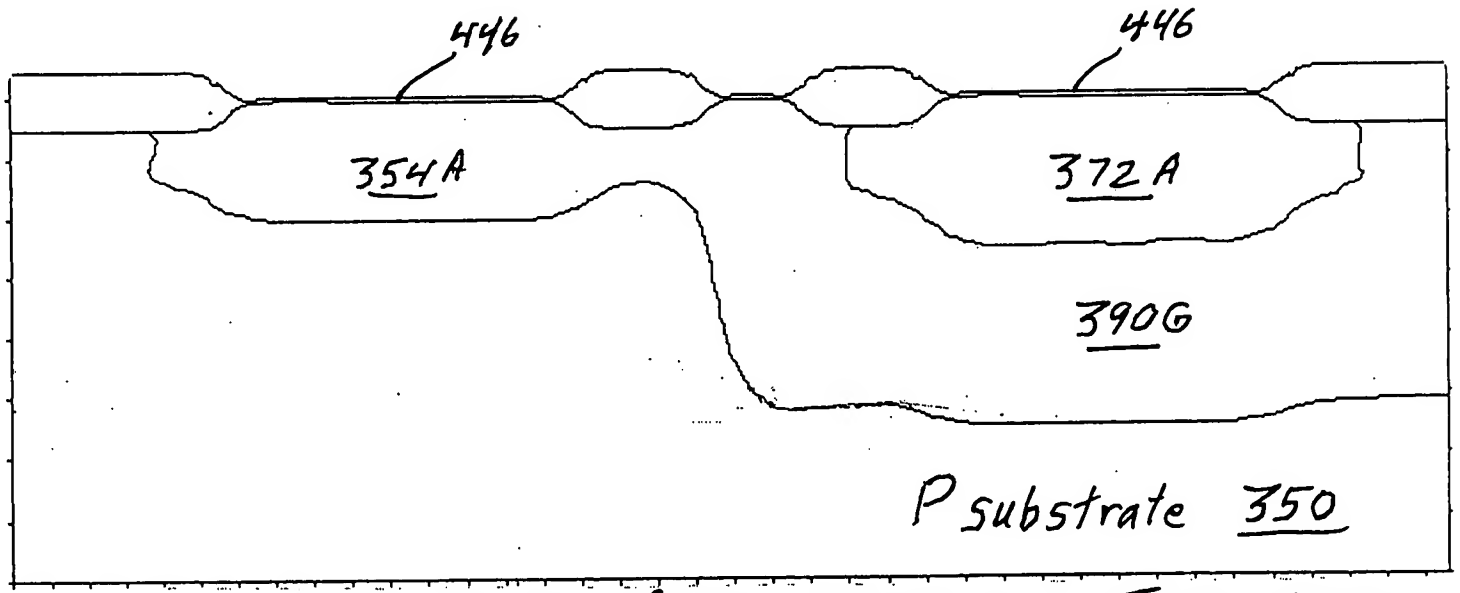


First Planar Gate Oxide

Fig 48E

5V PMOS 301

5V NMOS 302

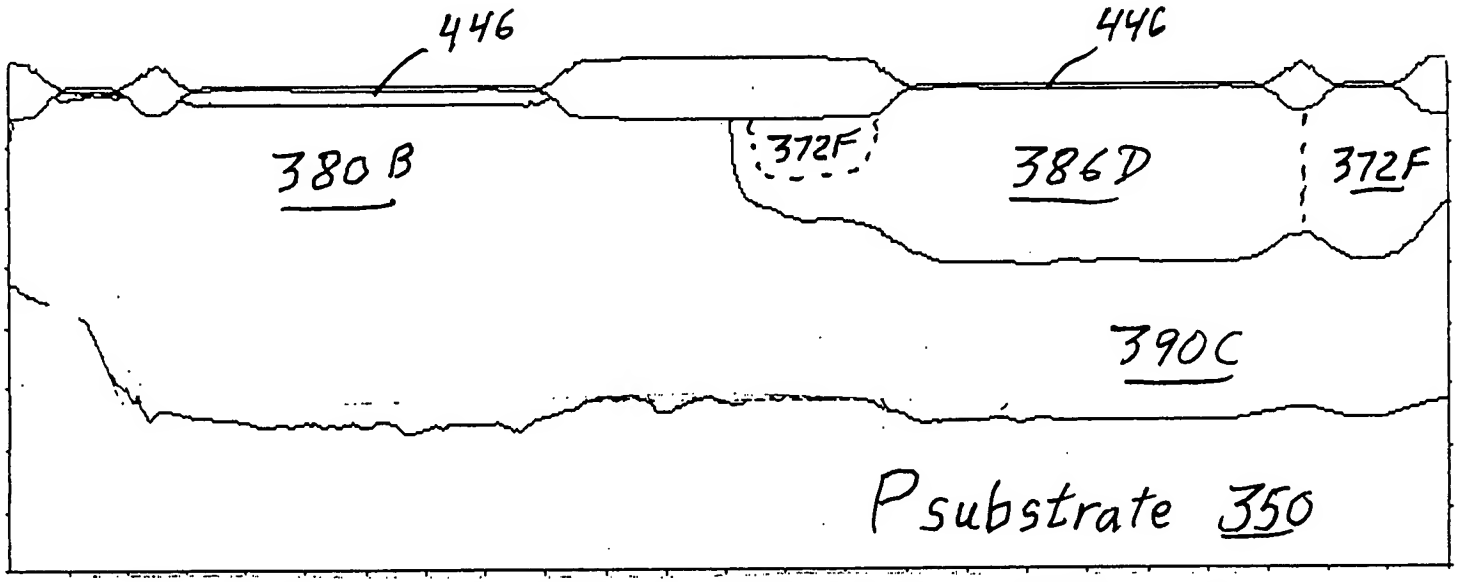


Threshold Adjust Implant - First Stage

Fig. 49A

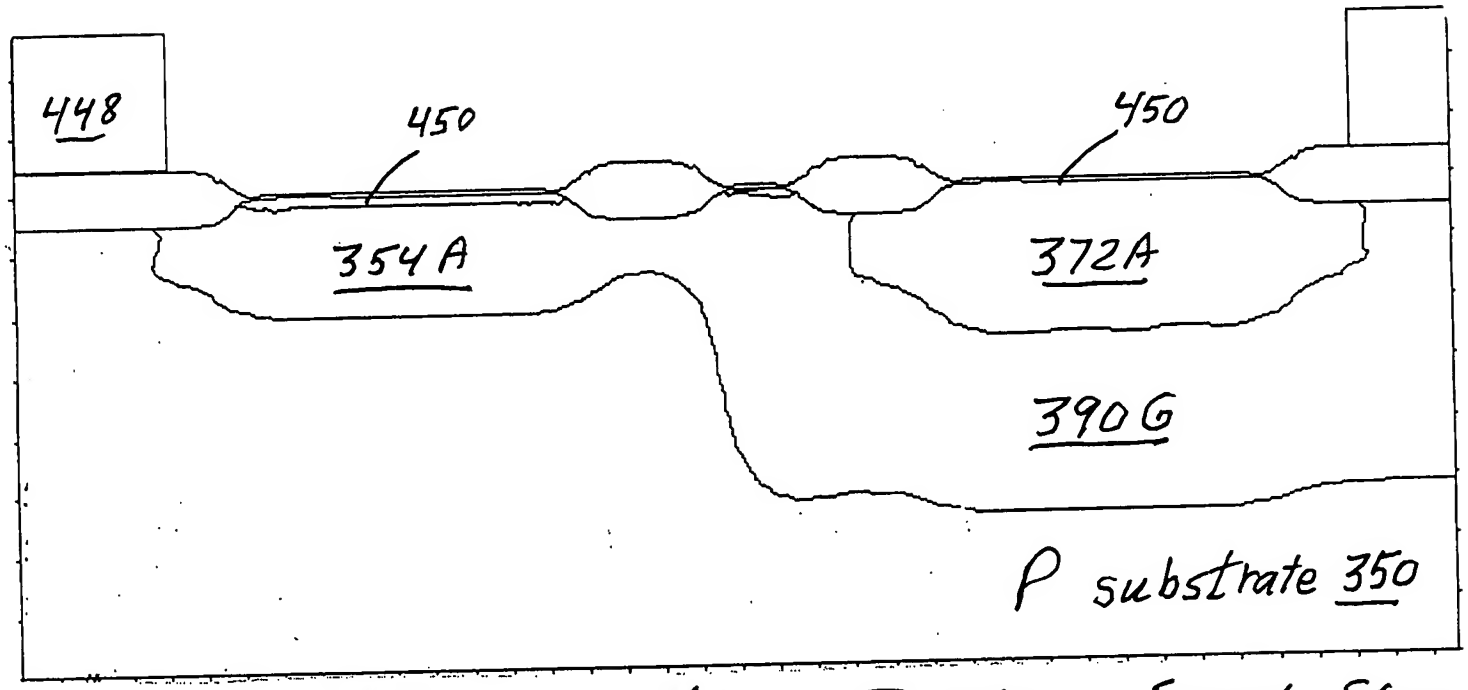
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Threshold Adjust Implant – First Stage

Fig. 49E

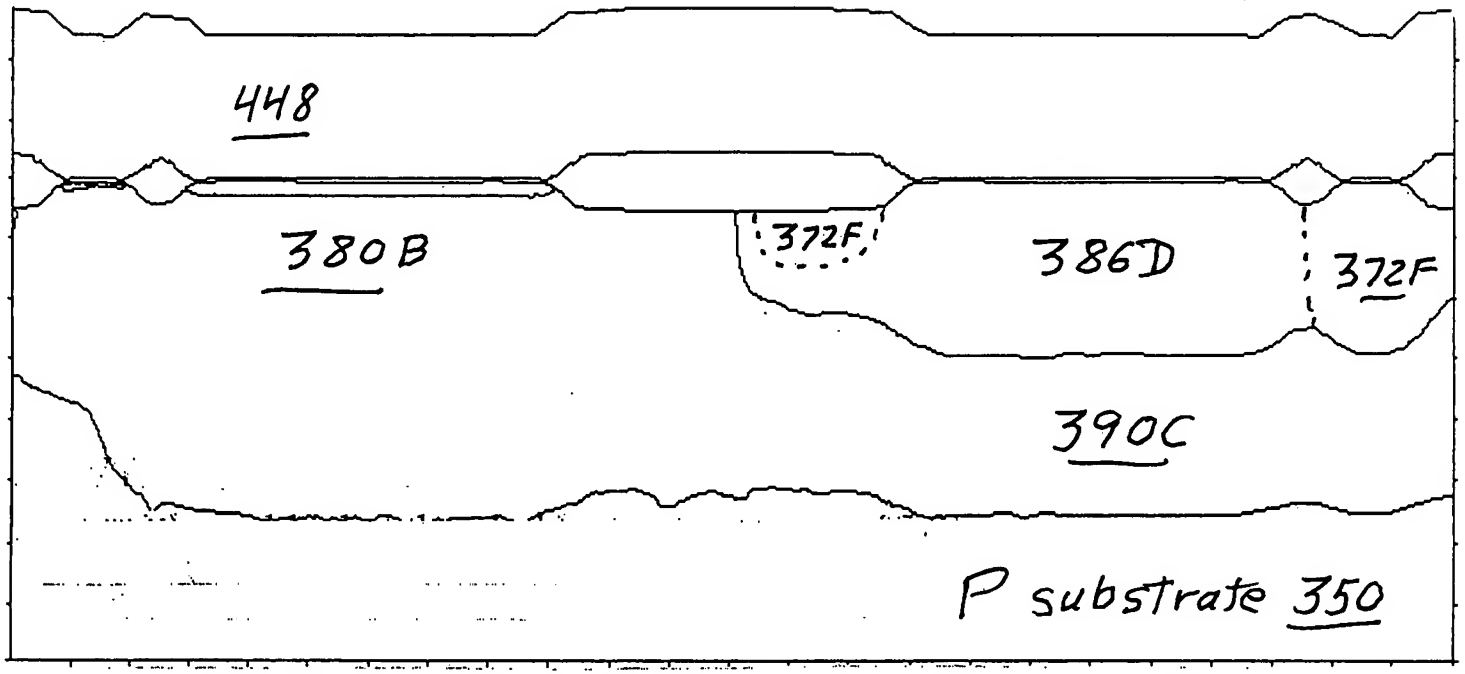


Threshold Adjust Implant – Second Stage
First Planar Gate Oxide Removal

Fig. 50A

Symmetrical 12V CMOS

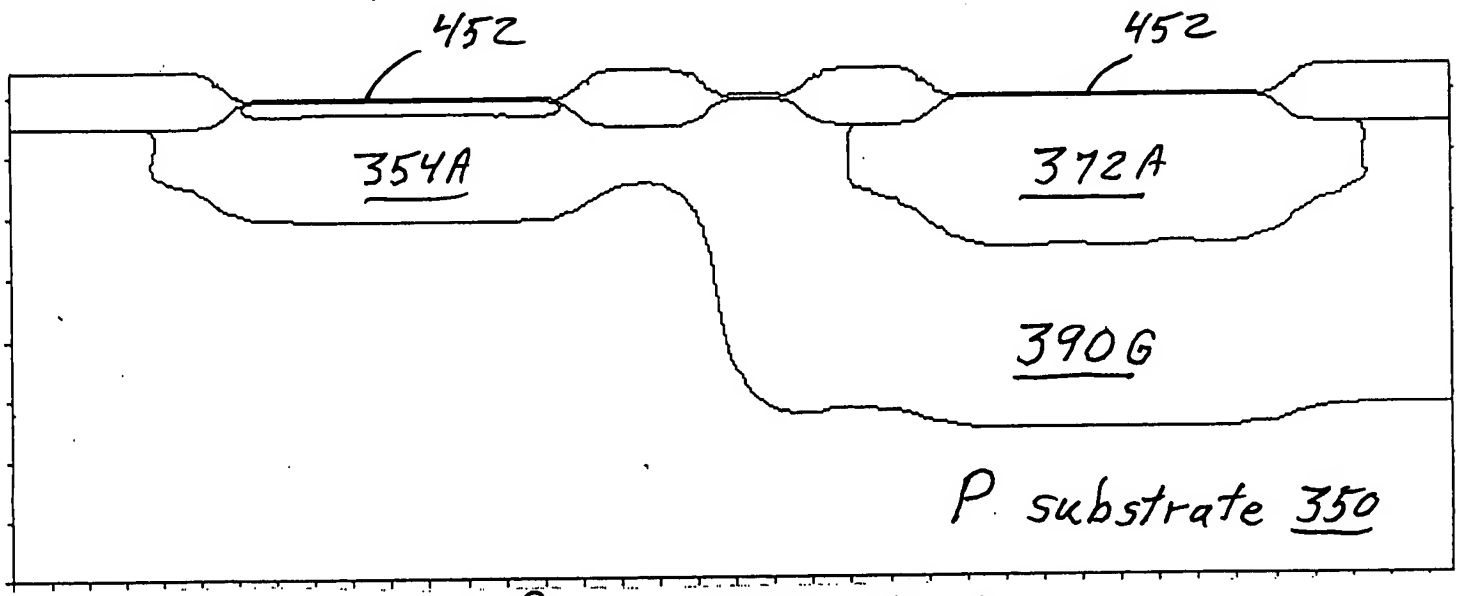
12V PMOS 309 12V NMOS 310



Threshold Adjust Implant - Second Stage

Fig. 50E

5V PMOS 301 5V NMOS 302

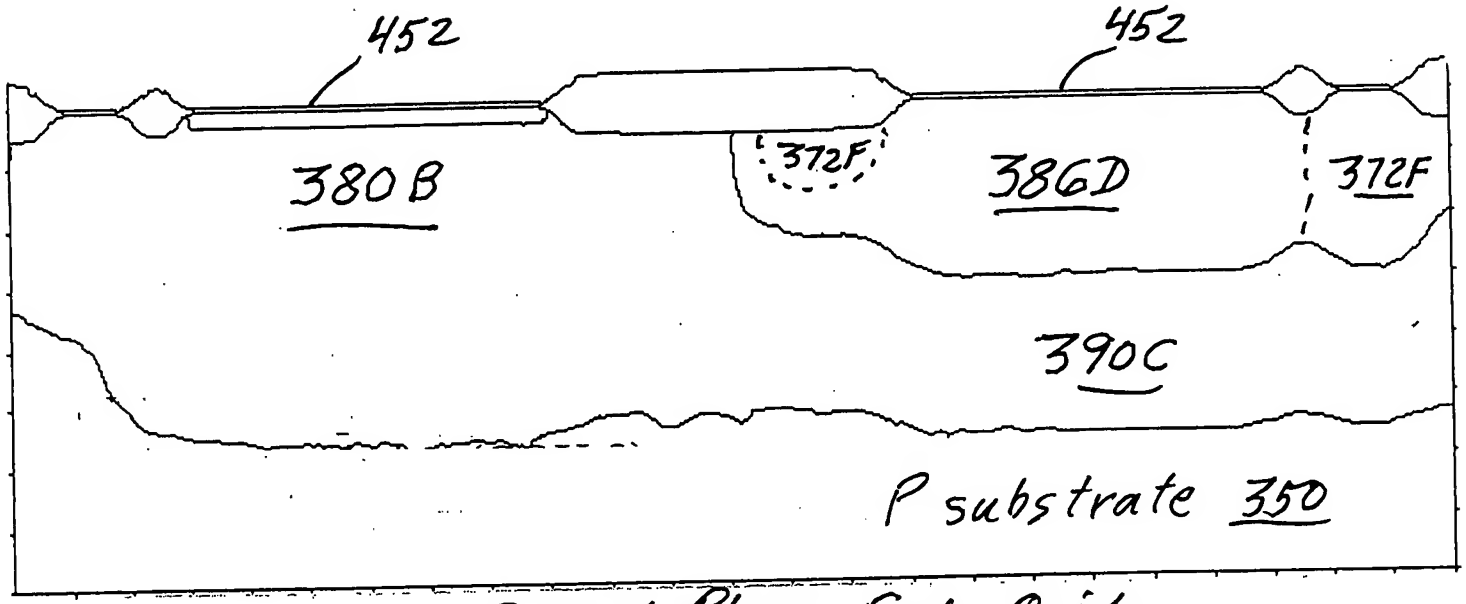


Second Planar Gate Oxide

Fig. 51A

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

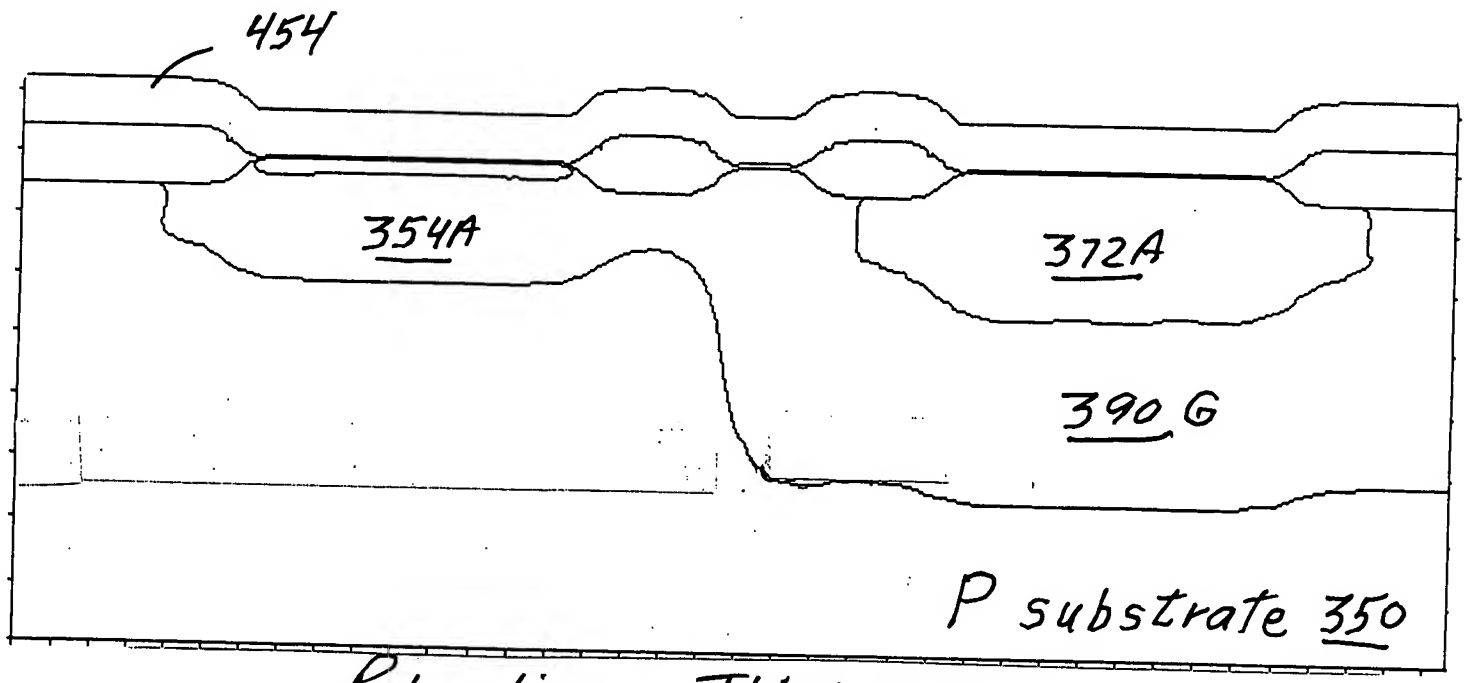


Second Planar Gate Oxide

Fig. 51E

5V PMOS 301

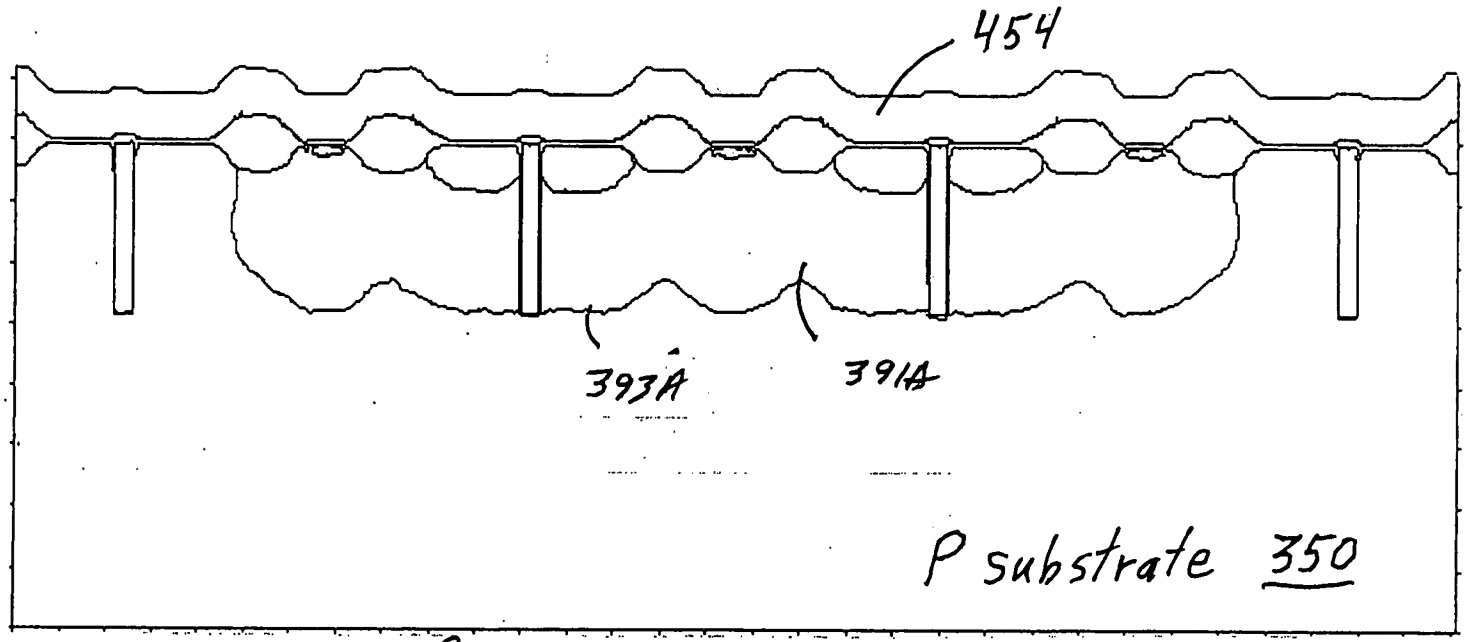
5V NMOS 302



Polysilicon - Third Layer

Fig. 52A

30V Lateral Trench DMOS 308

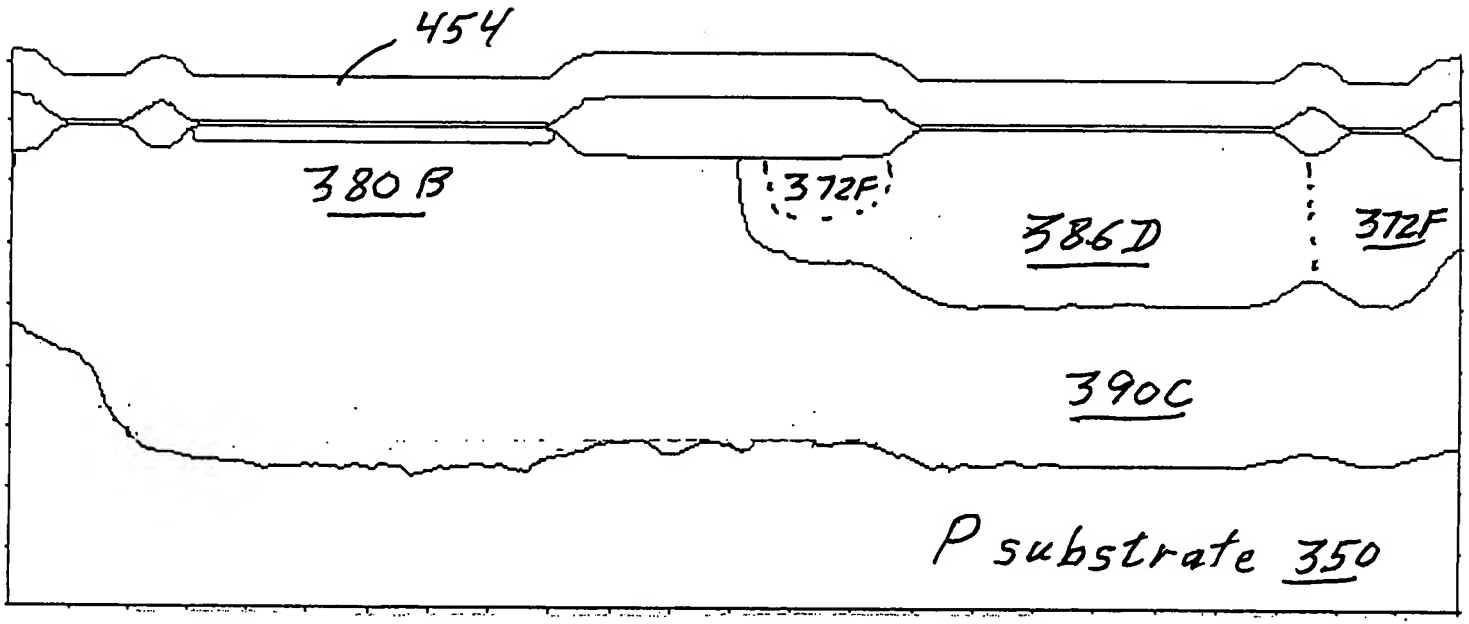


Polysilicon – Third Layer

Fig. 52D

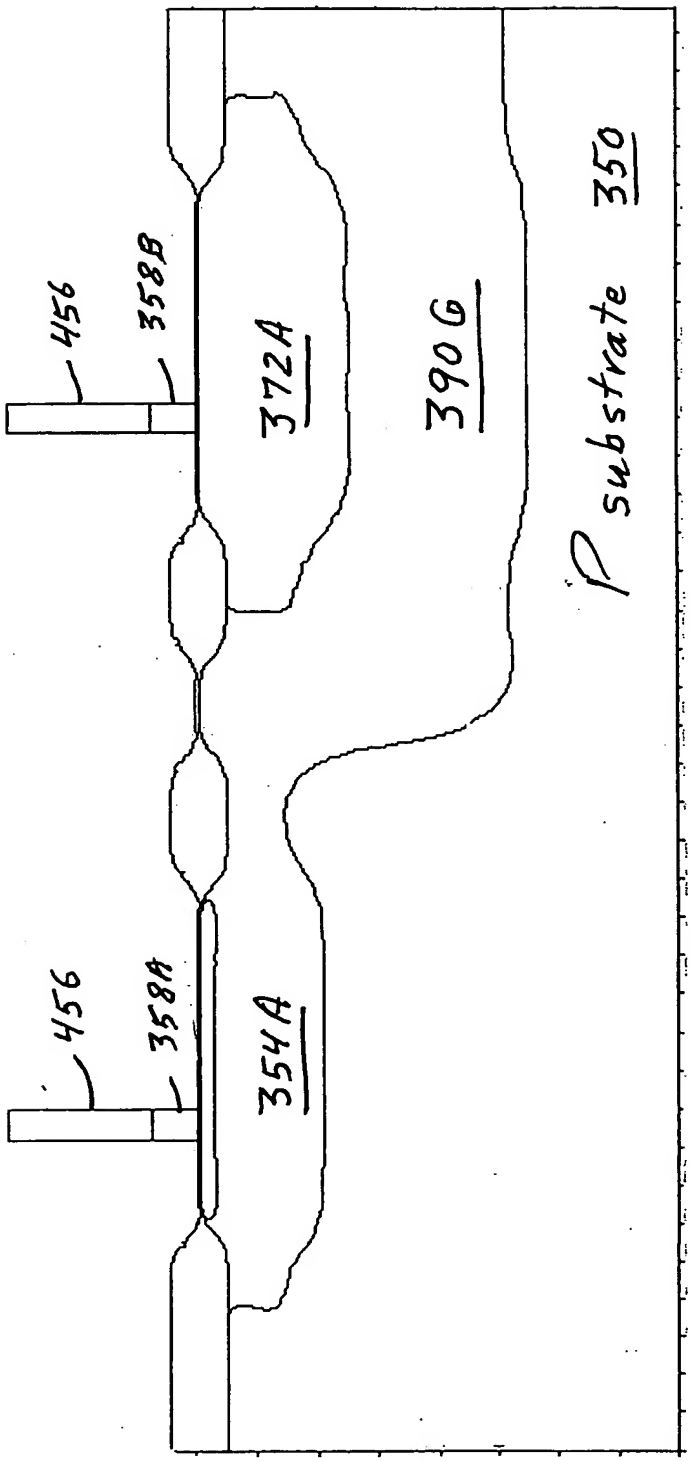
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Polysilicon - Third Layer

Fig. 52E



Planar Gate Formation
Fig. 5"3A

30V Lateral Trench DMOS 308

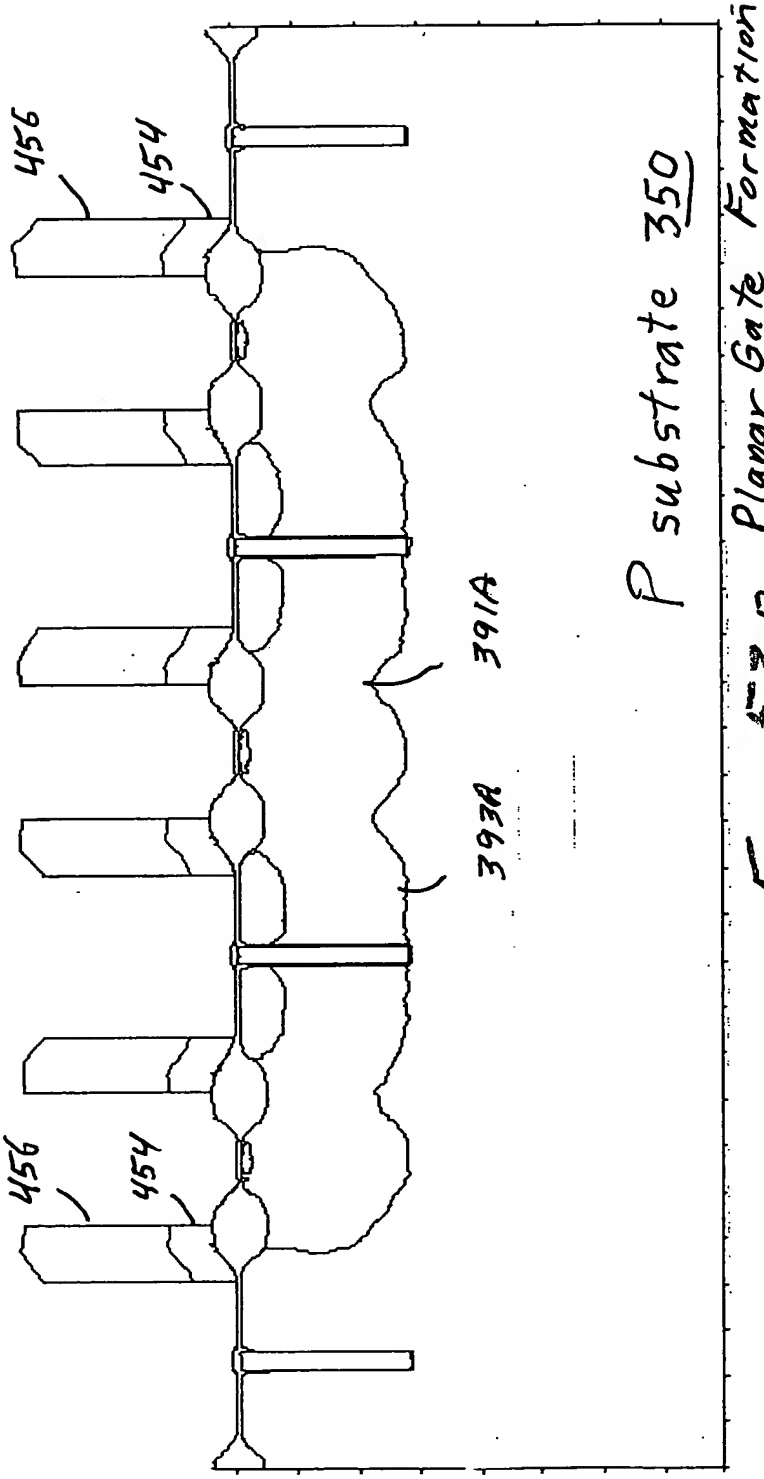
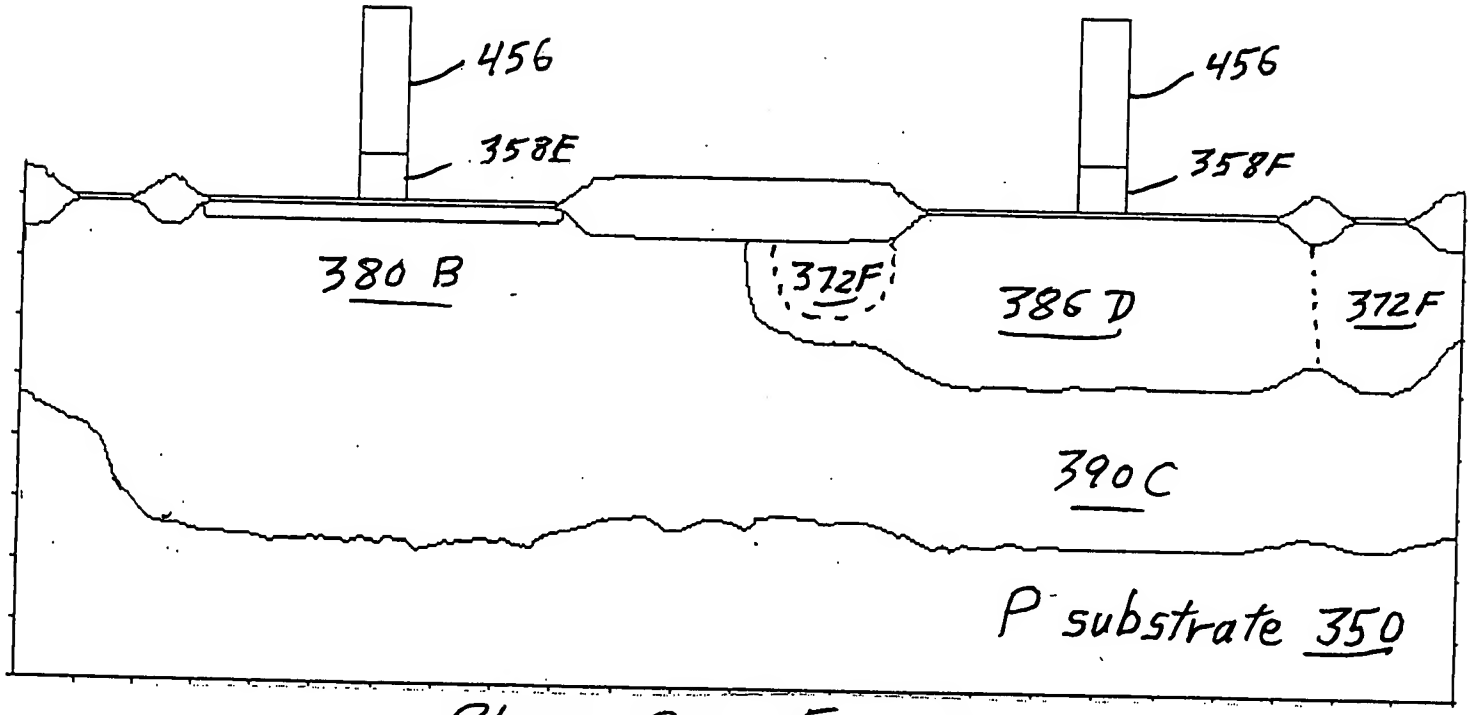


Fig. 3D Planar Gate Formation

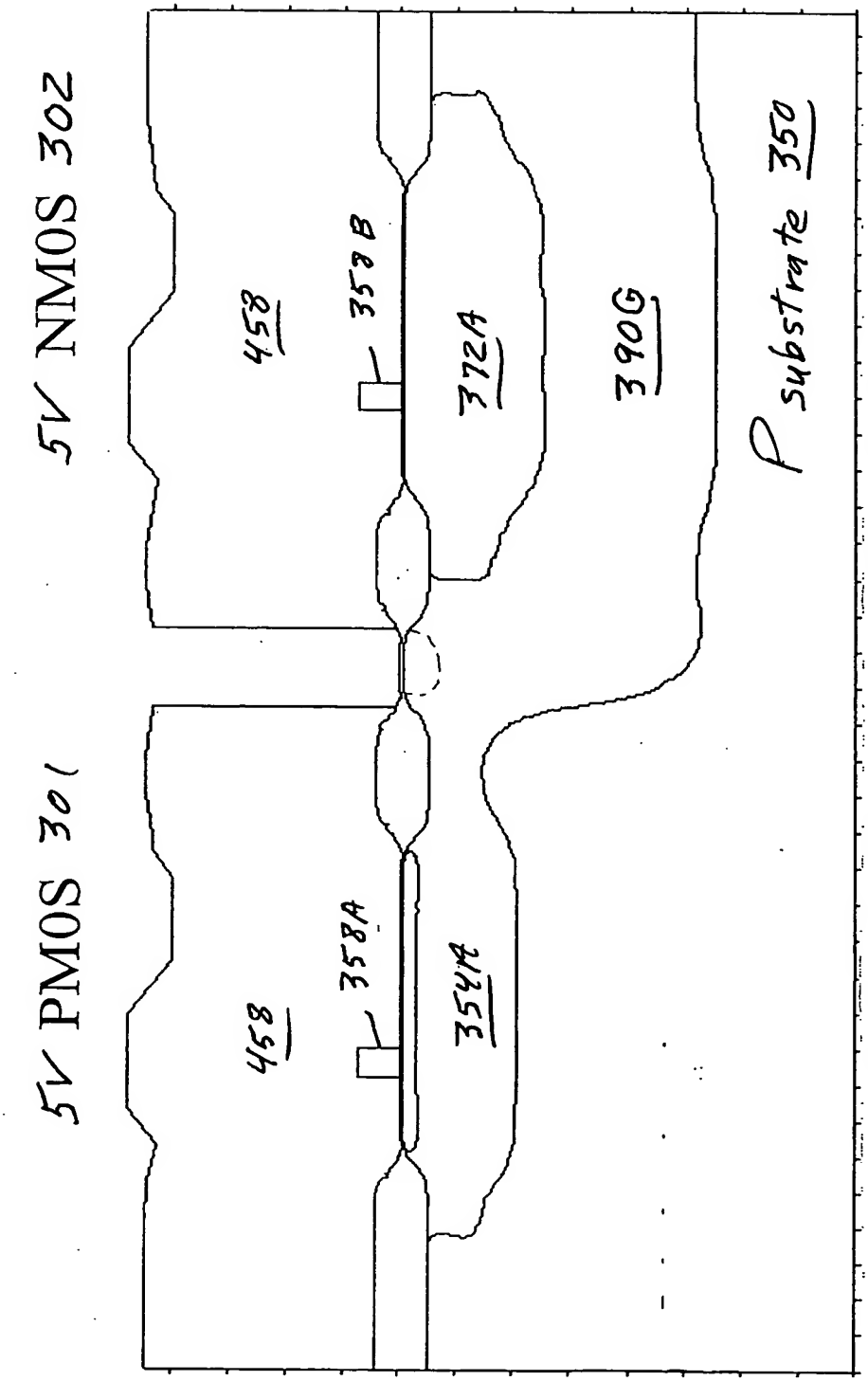
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Planar Gate Formation

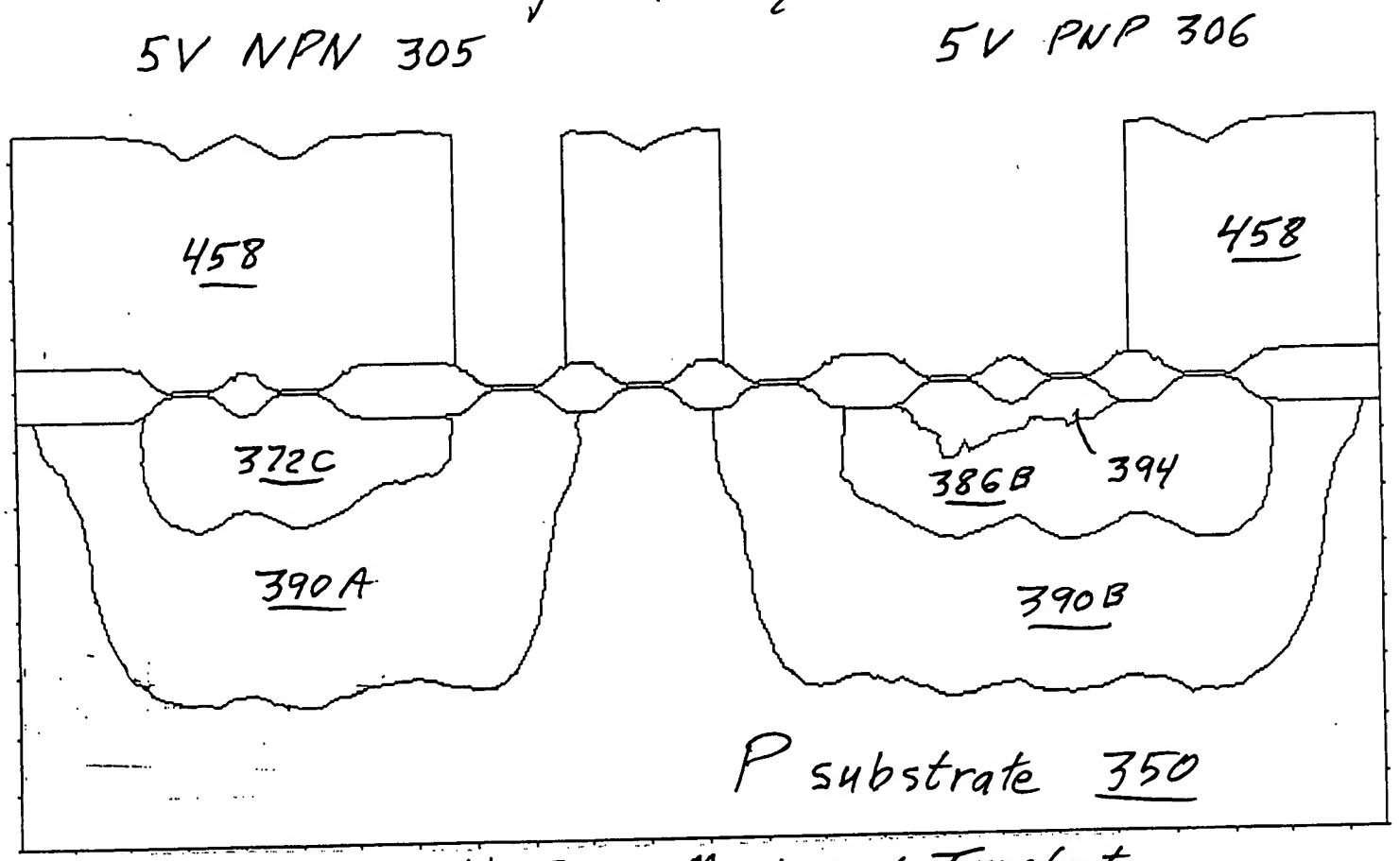
Fig 53E



N-Base Mask and Implant

Fig. 54D

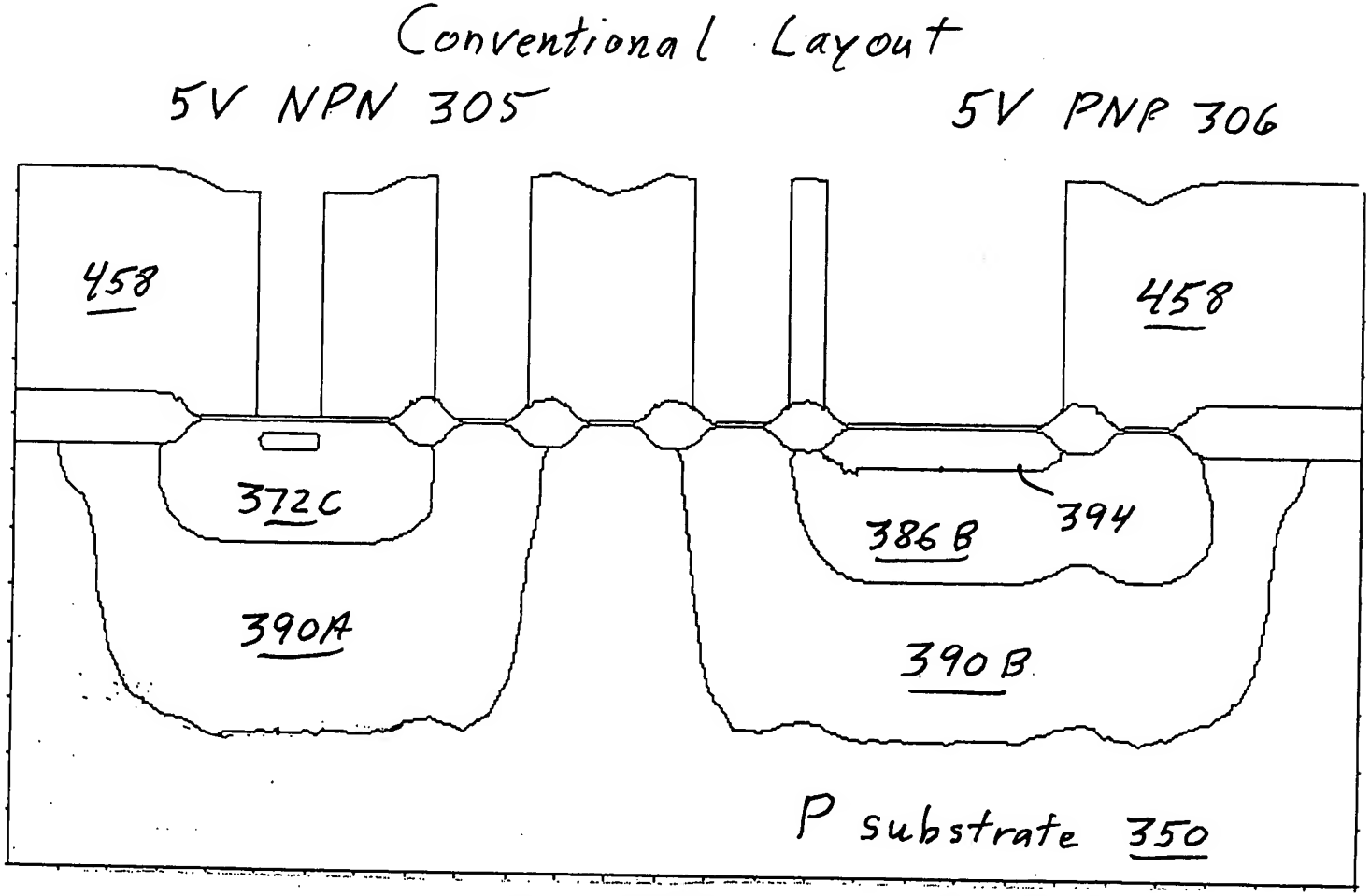
High F_T Layout



N-Base Mask and Implant

Fig. 54B

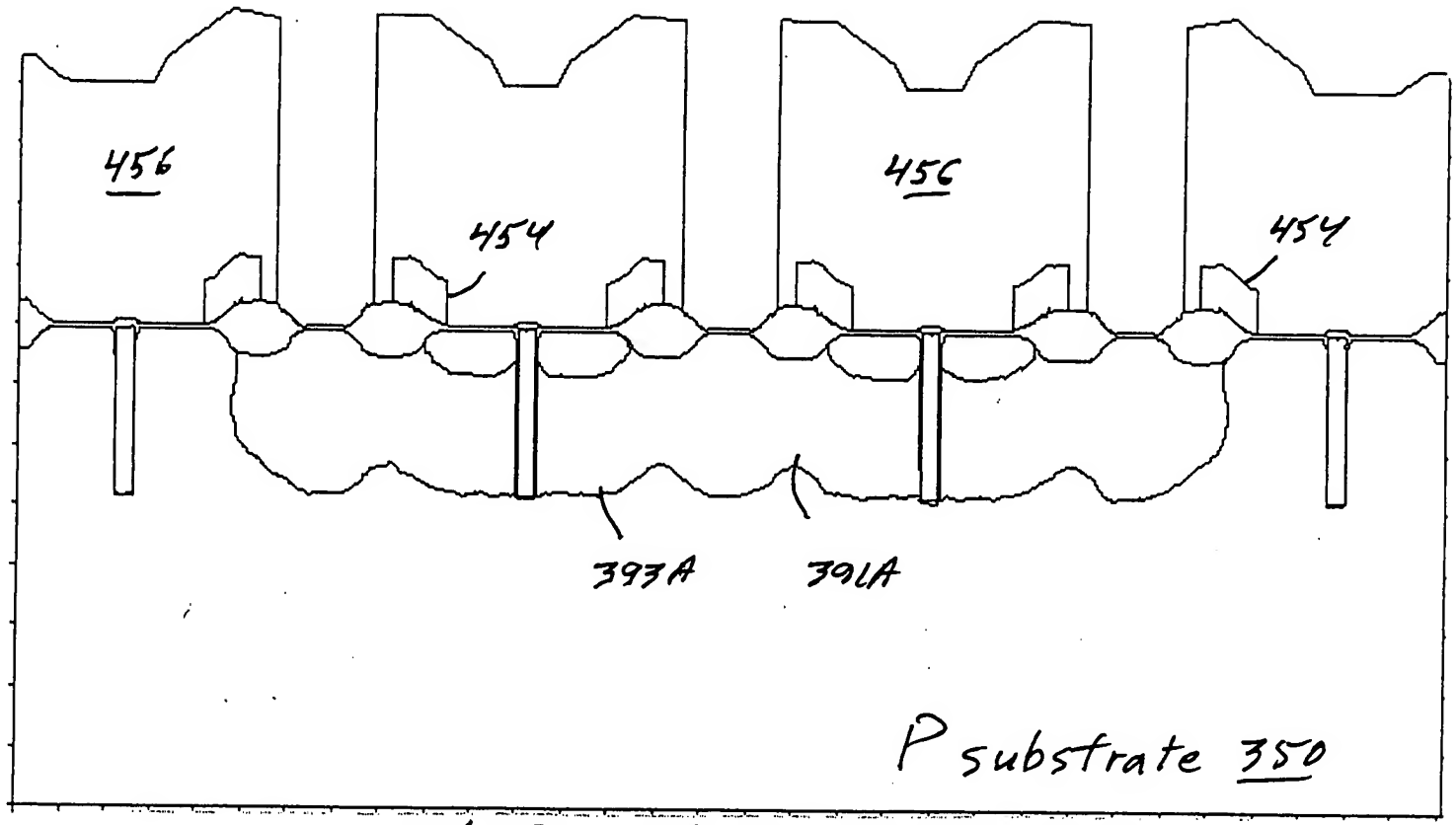
Conventional Layout



N-Base Mask and Implant

Fig. 54C

30V Lateral Trench DMOS 308

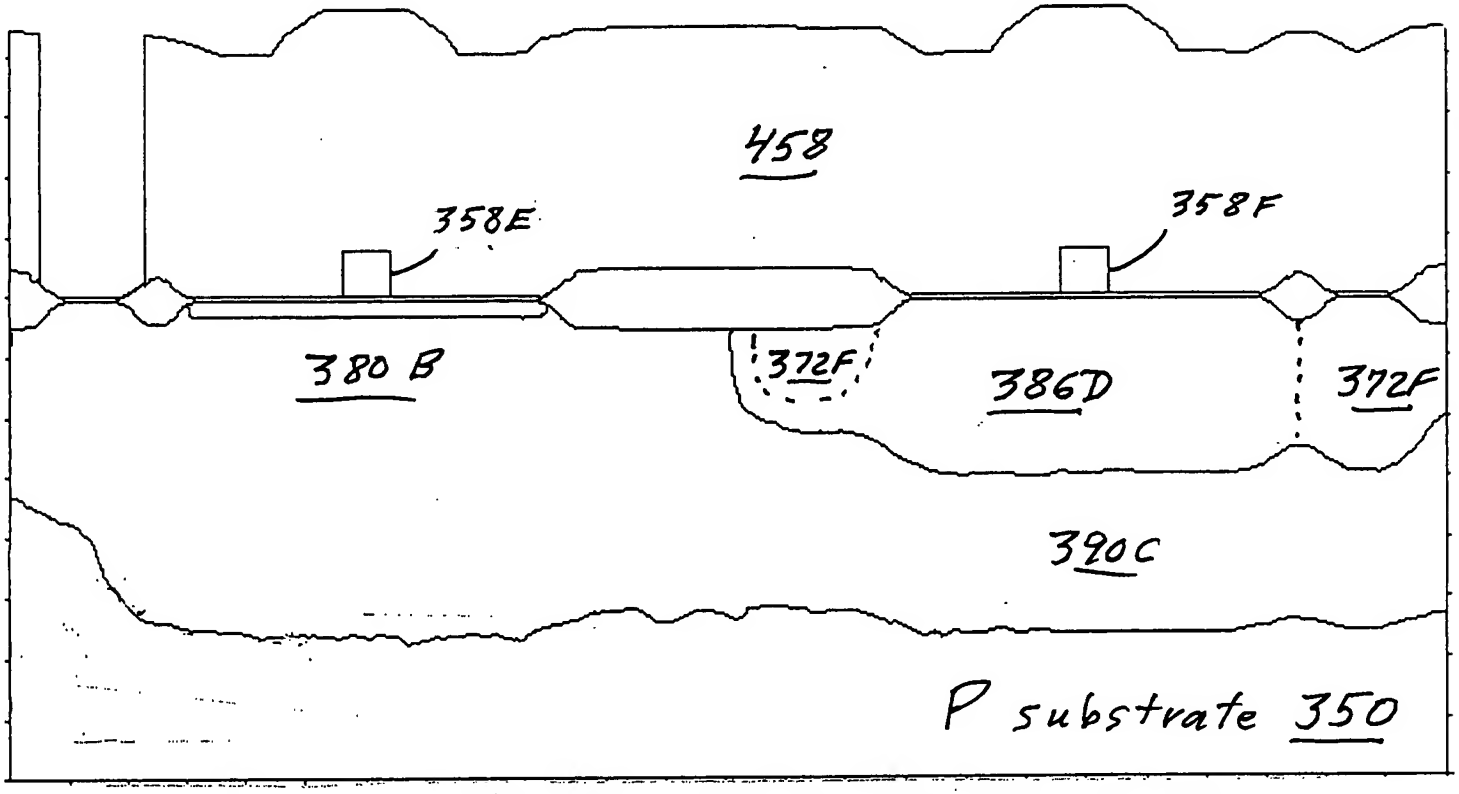


N-Base Mask and Implant

Fig. 54D

Symmetrical 12V CMOS

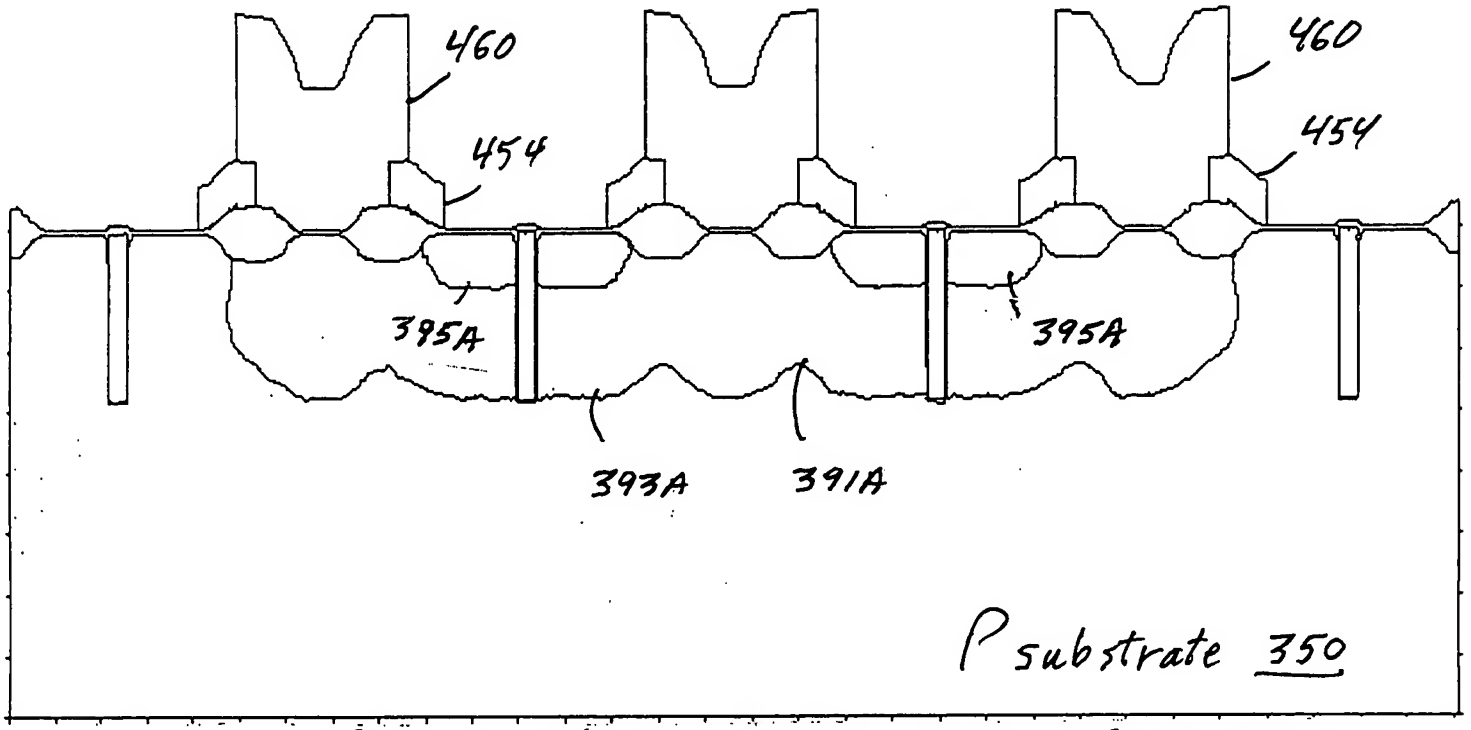
12V PMOS 309 12V NMOS 310



N- Base Mask and Implant

Fig. 54E

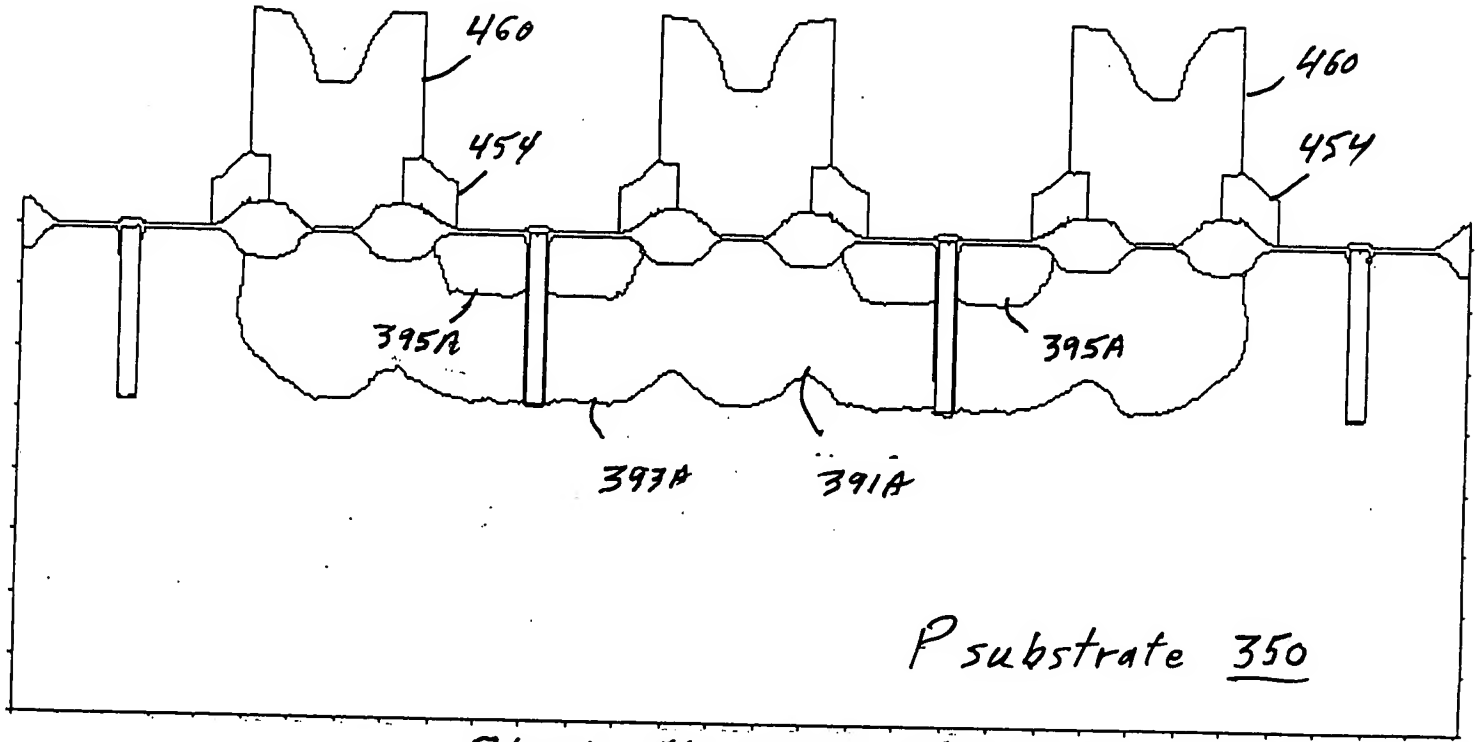
30V Lateral Trench DMOS 308



P Body Mask and Implant - First Stage

Fig. 5D

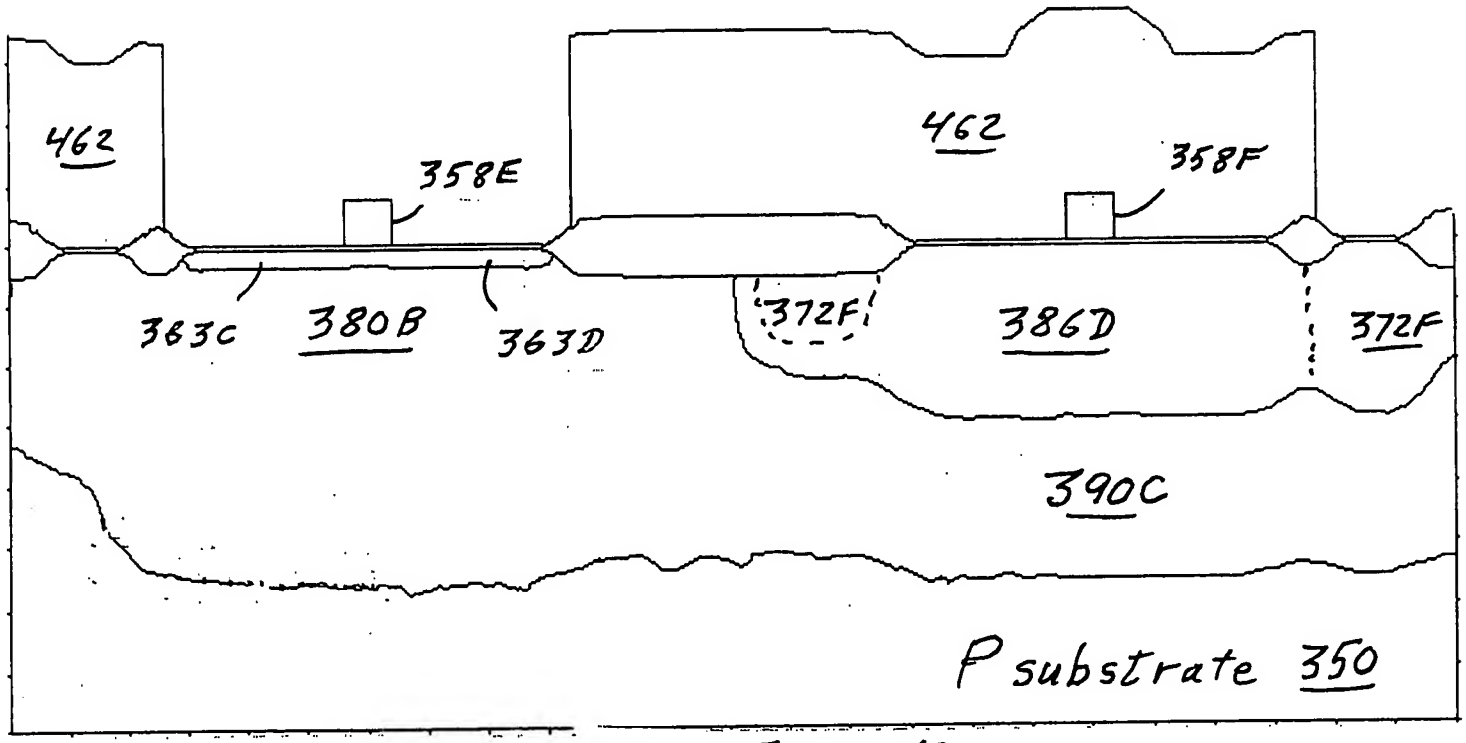
30V Lateral Trench DMOS 308



Pbody Mask and Implant - Second Stage
Fig. 56D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

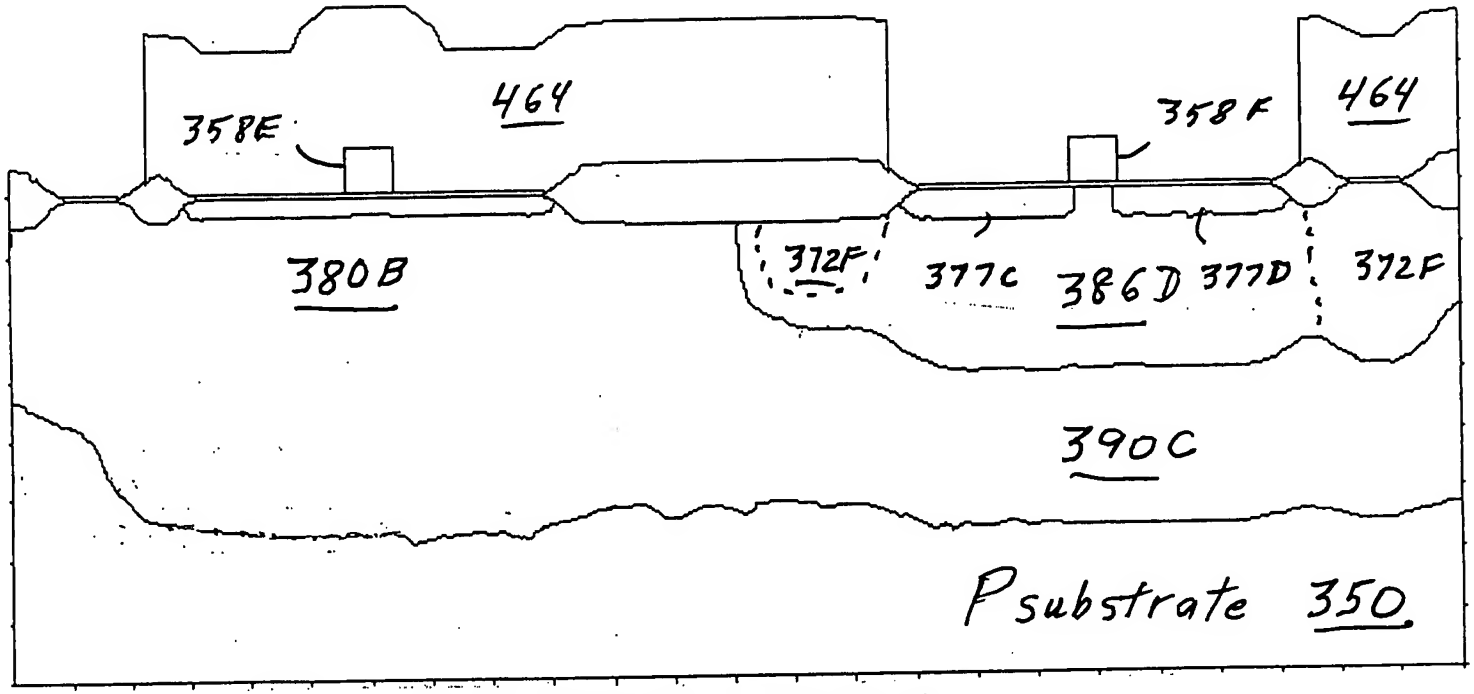


12V P-LDD Implant

Fig. 57E

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



12V N-LDD Implant

Fig. 58E

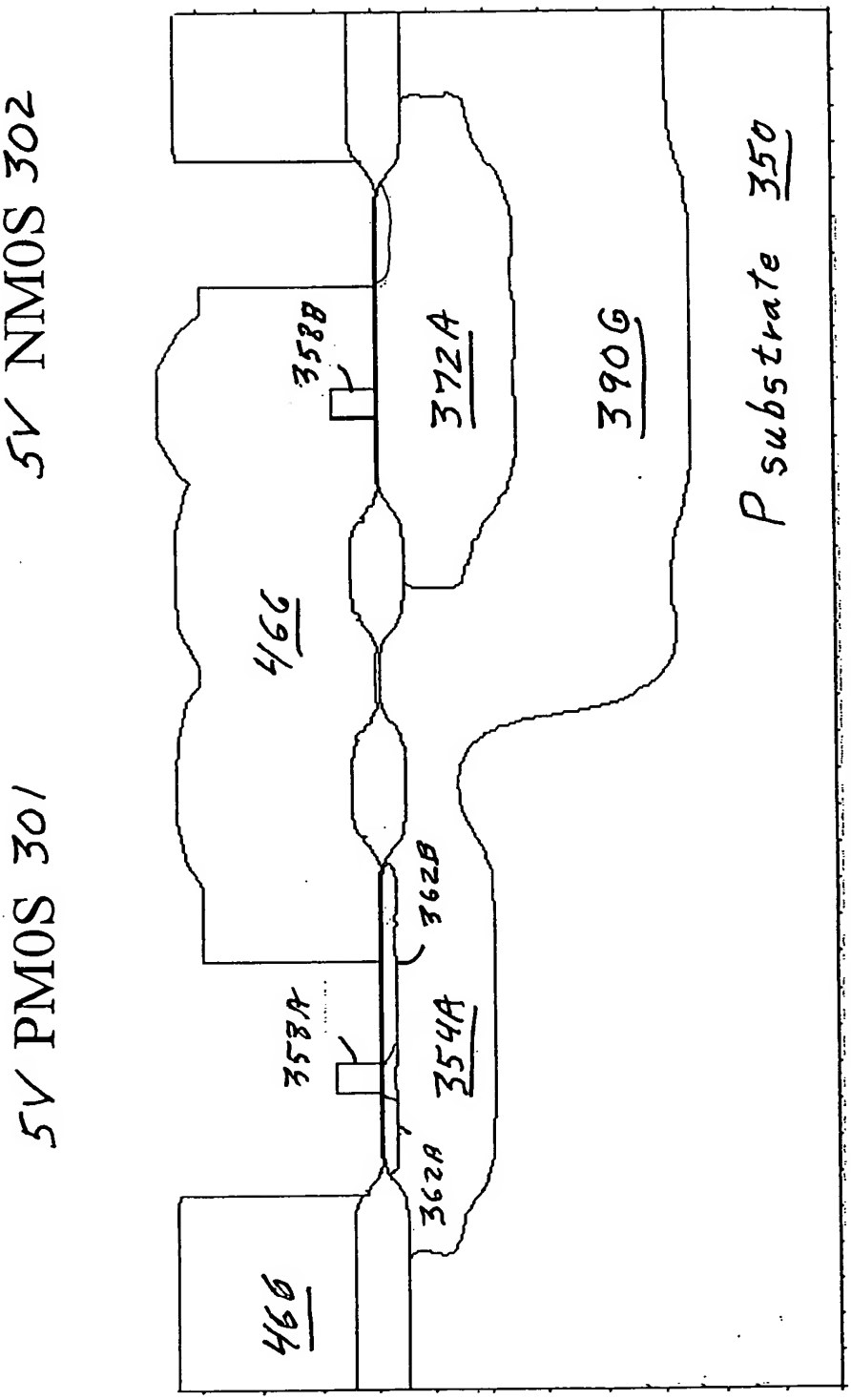
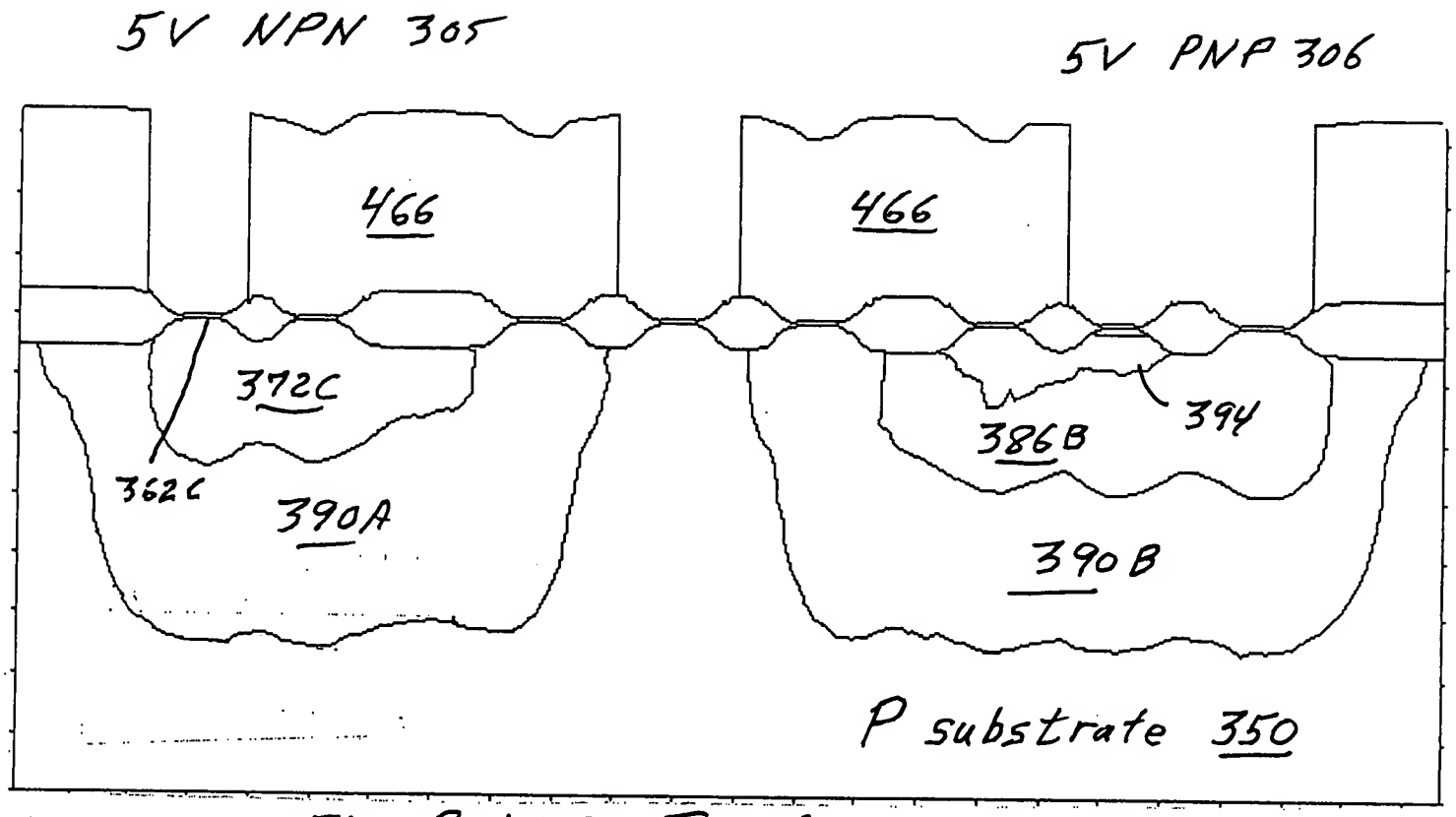

5V NMOS 302
5V PMOS 301
358B
372A
390G
P substrate 350
416
362B
358A
354A
362A
466
5V P-LDD Implant

FIG. 5PA

High F_T Layout



5V P-LDD Implant

Fig 59B

Conventional Layout

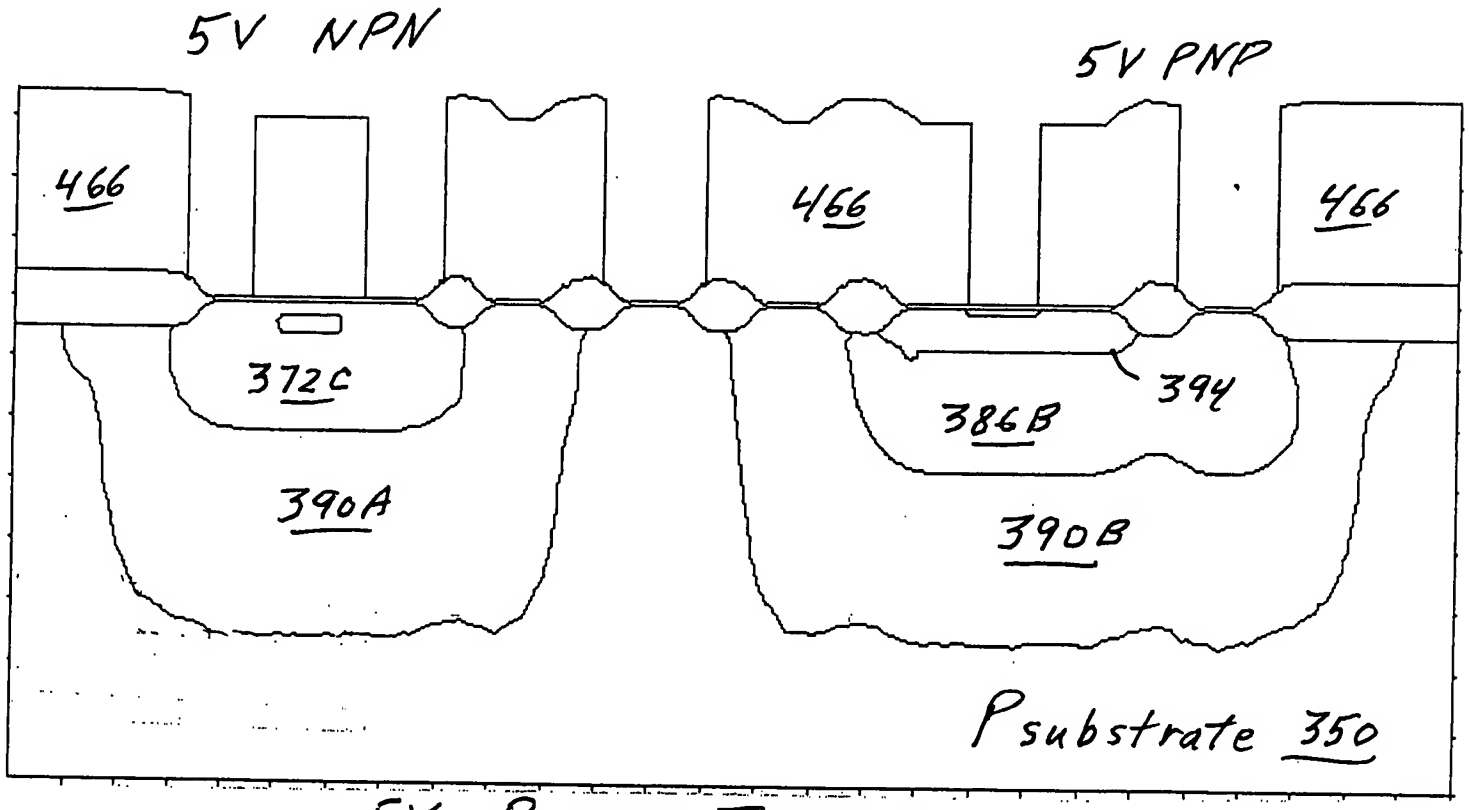
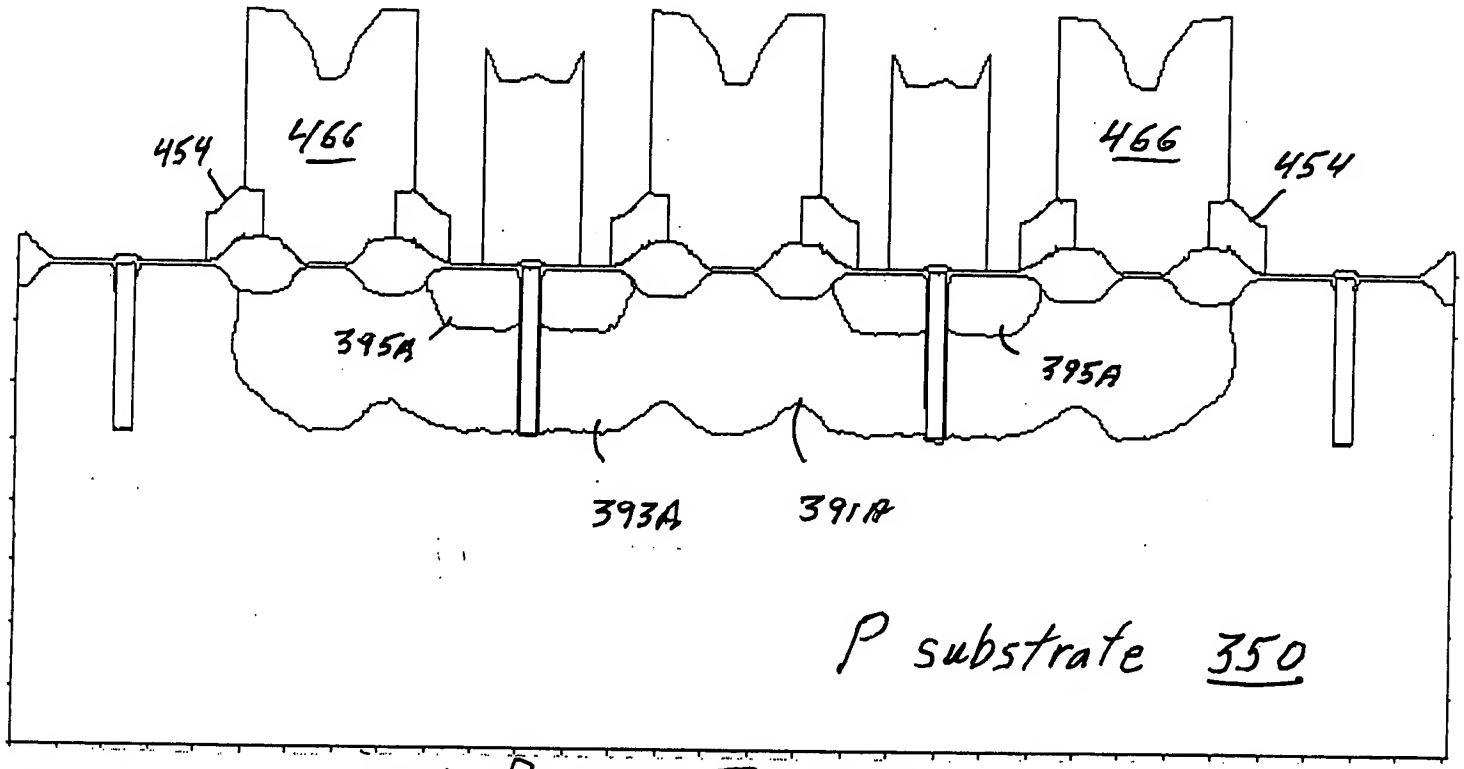


Fig. 59C

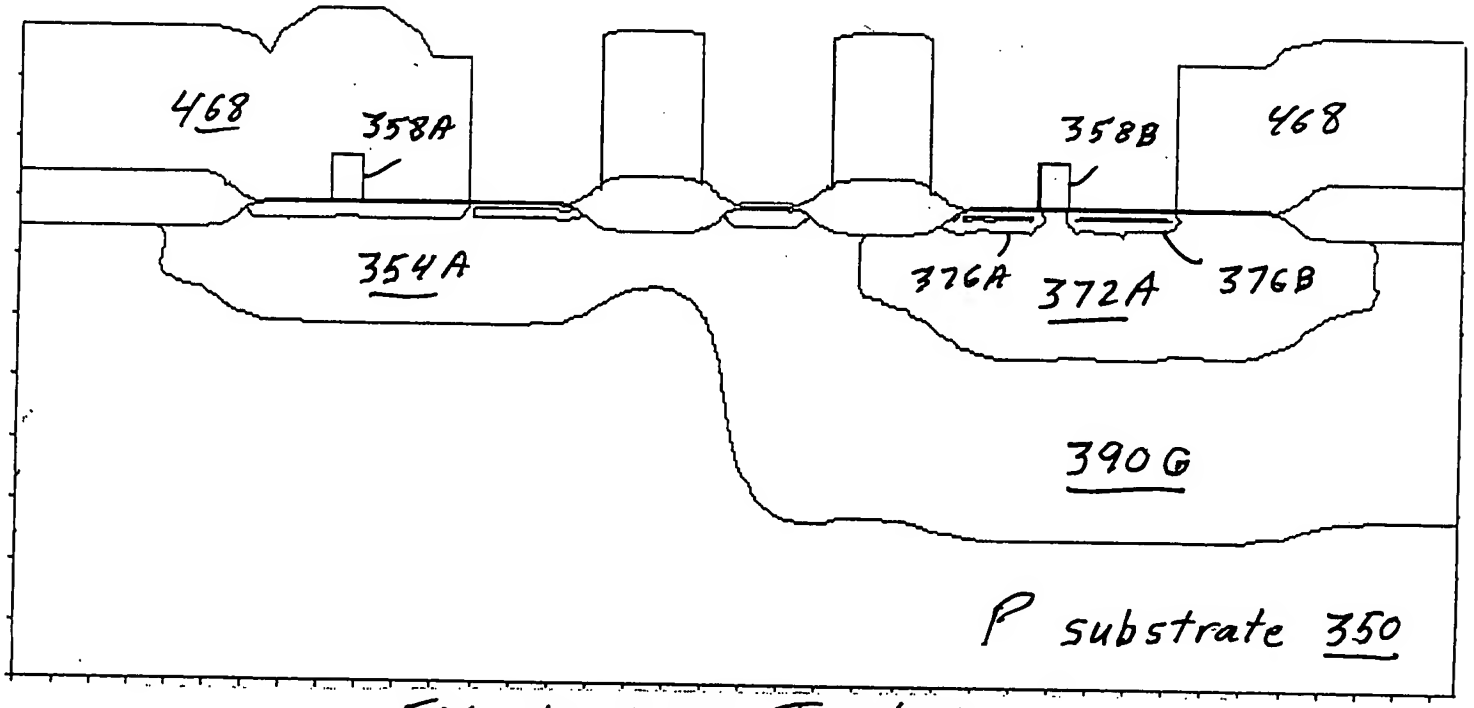
30V Lateral Trench DMOS 308



5V P-LDD Implant

Fig. 59D

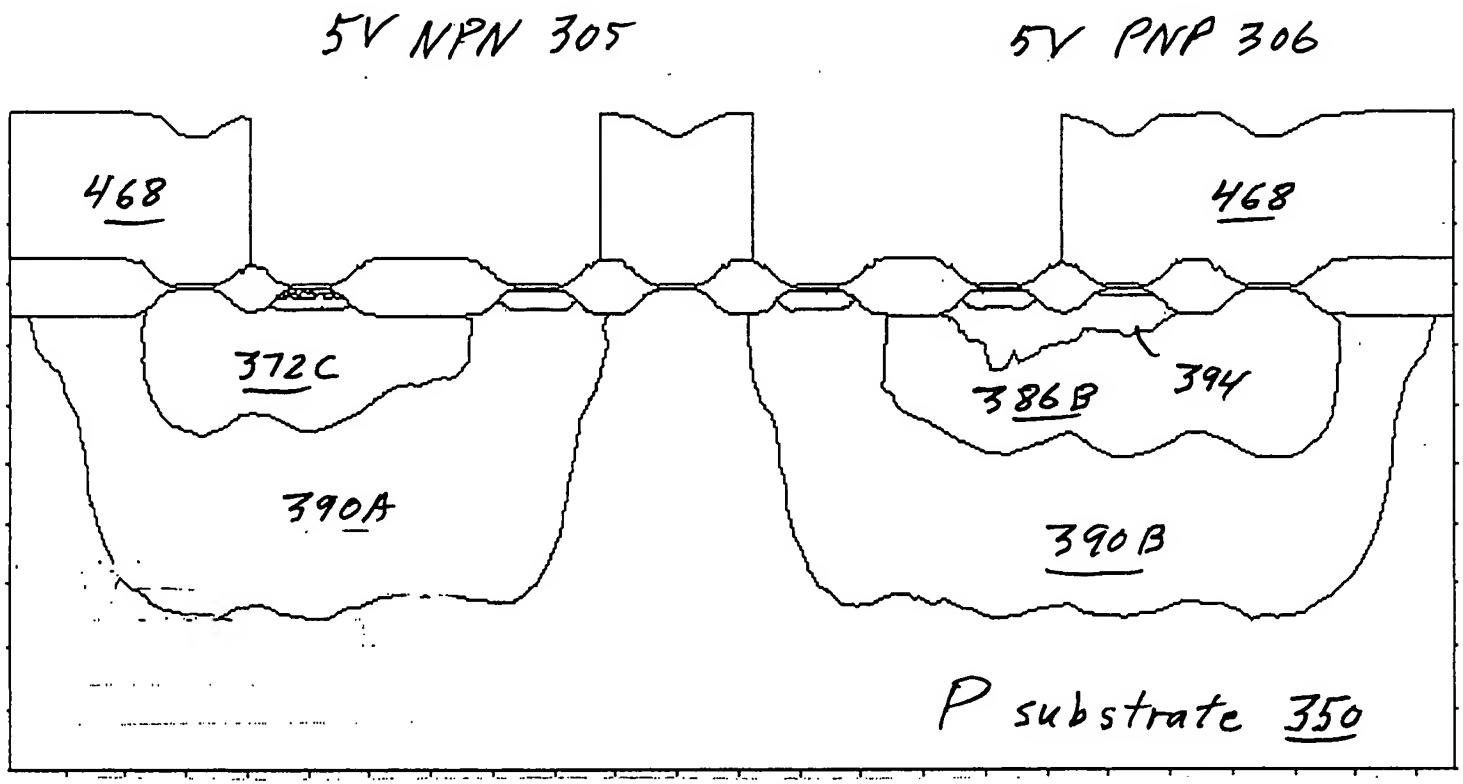
5V PMOS 301 5V NMOS 302



5V N-LDD Implant

Fig. 60A

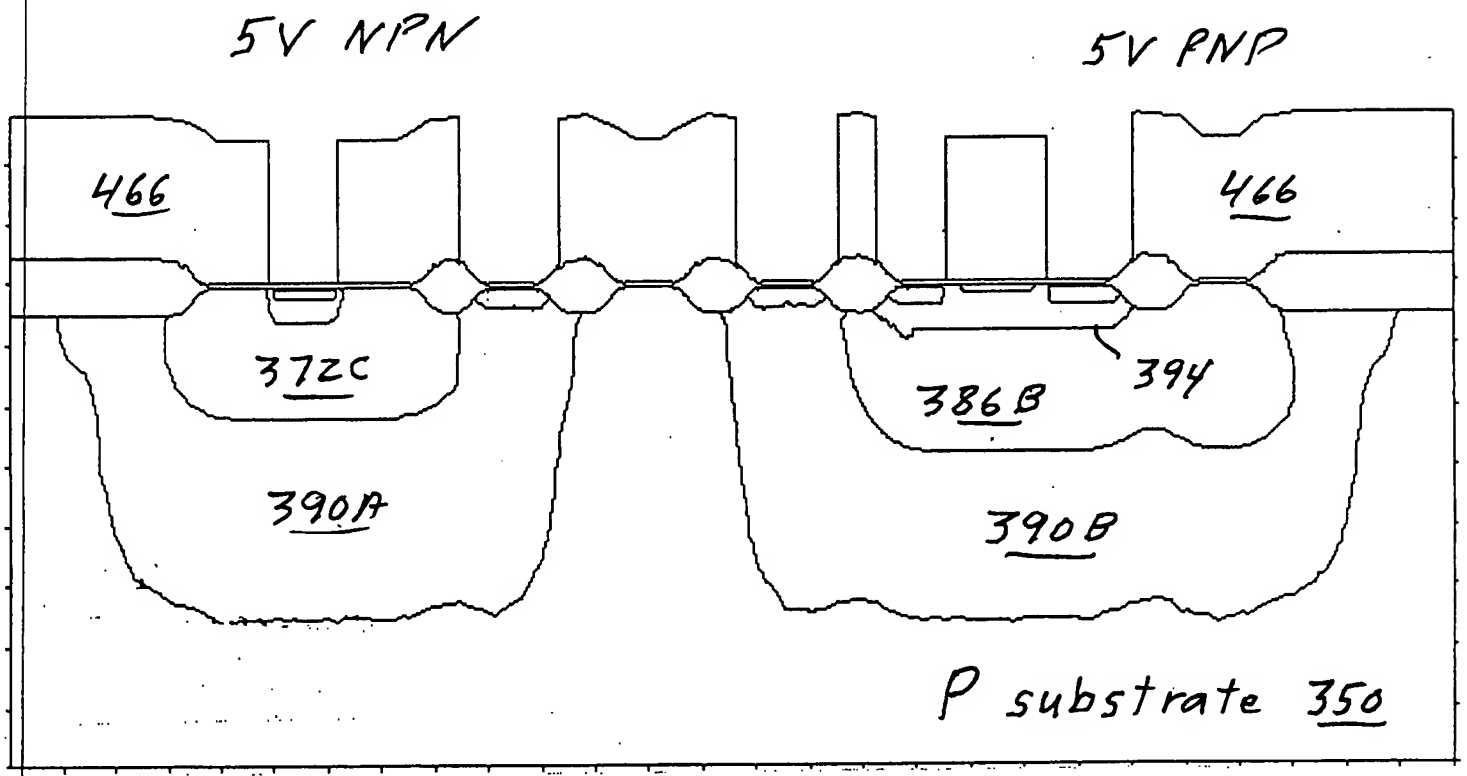
High F_T Layout



5V N-LDD Implant

Fig 6OB

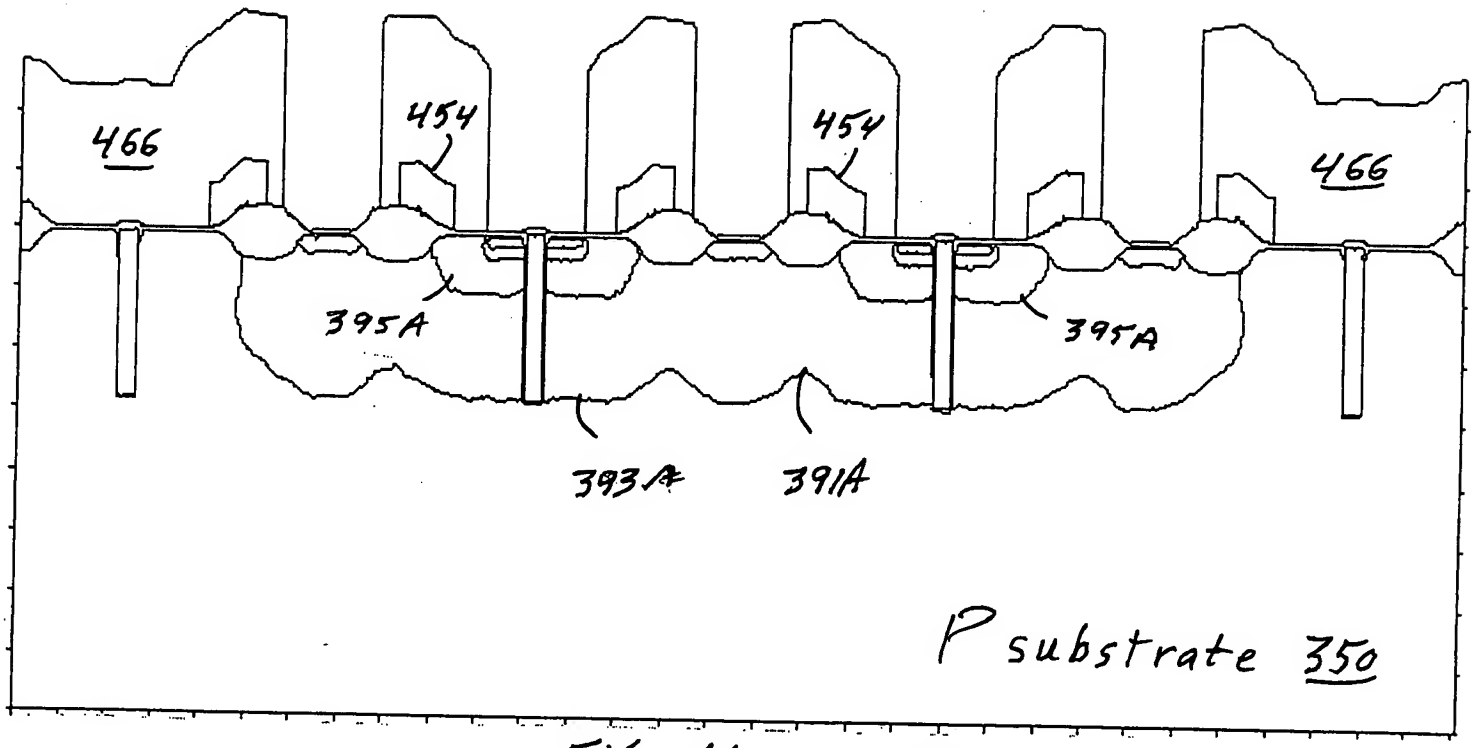
Conventional Layout



5V N-LDD Implant

Fig. 60C

30V Lateral Trench DMOS 308



5V N-LDD Implant

Fig. 60D

612/181

5V PMOS 301 5V NMOS 302

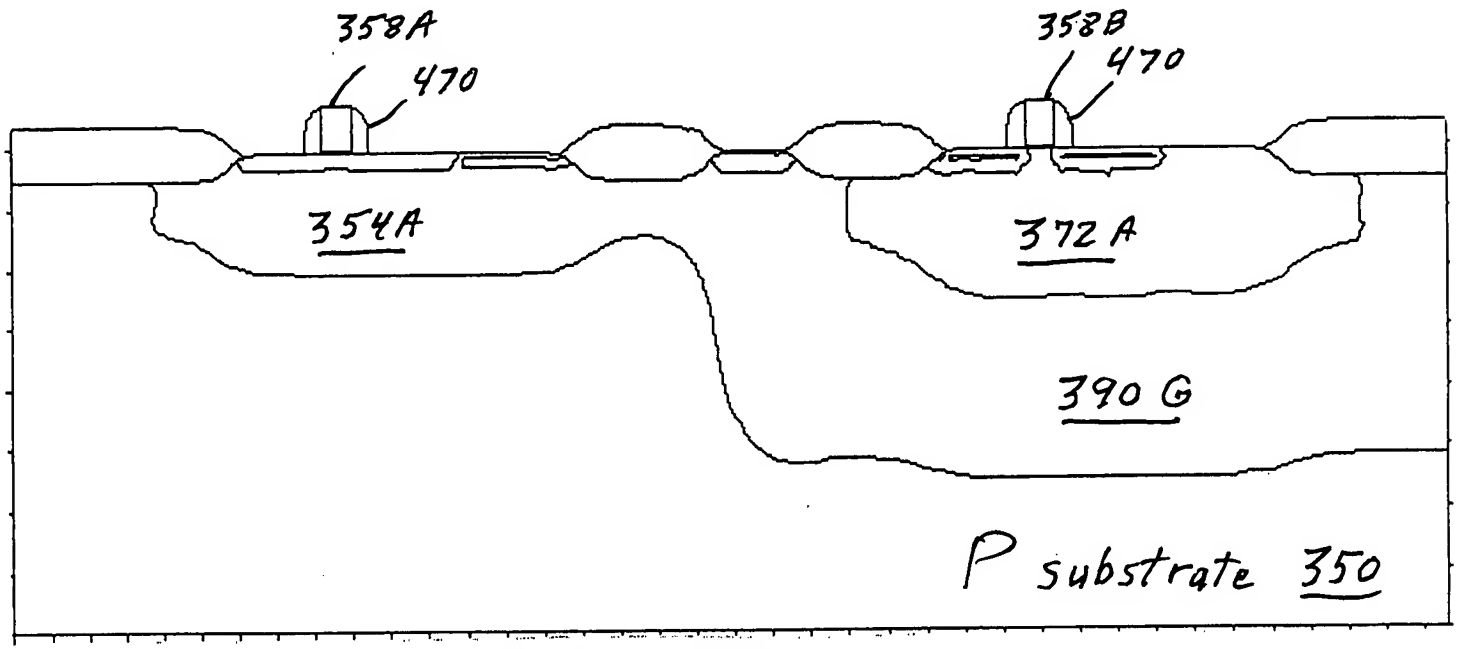


Fig. 6lA

30V Lateral Trench DMOS 308

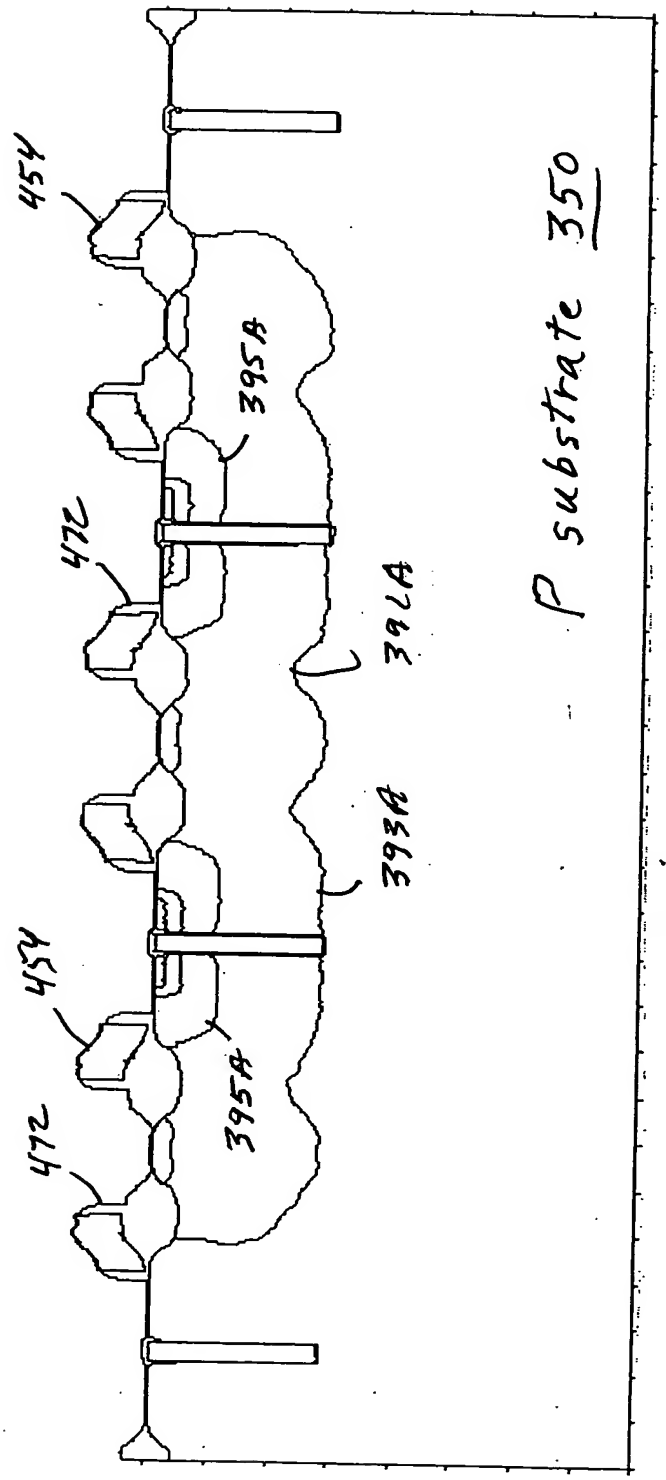
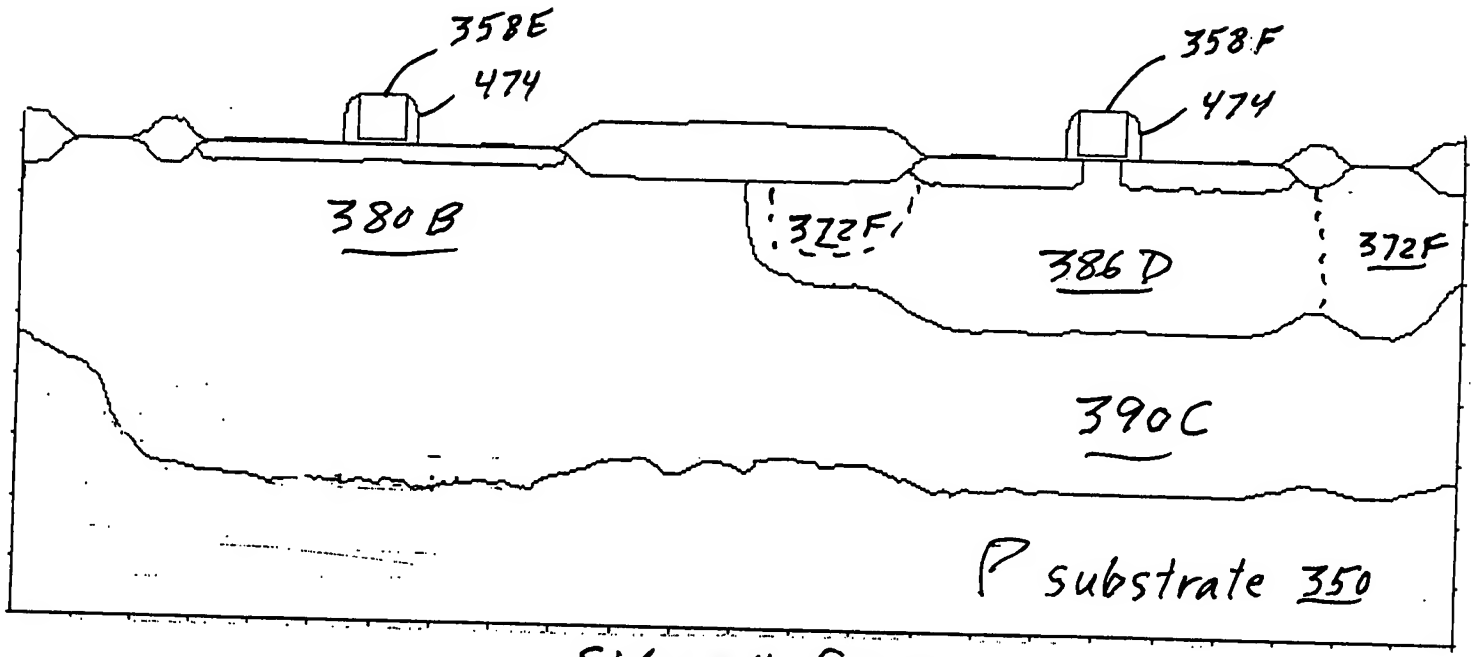


Fig. 6D

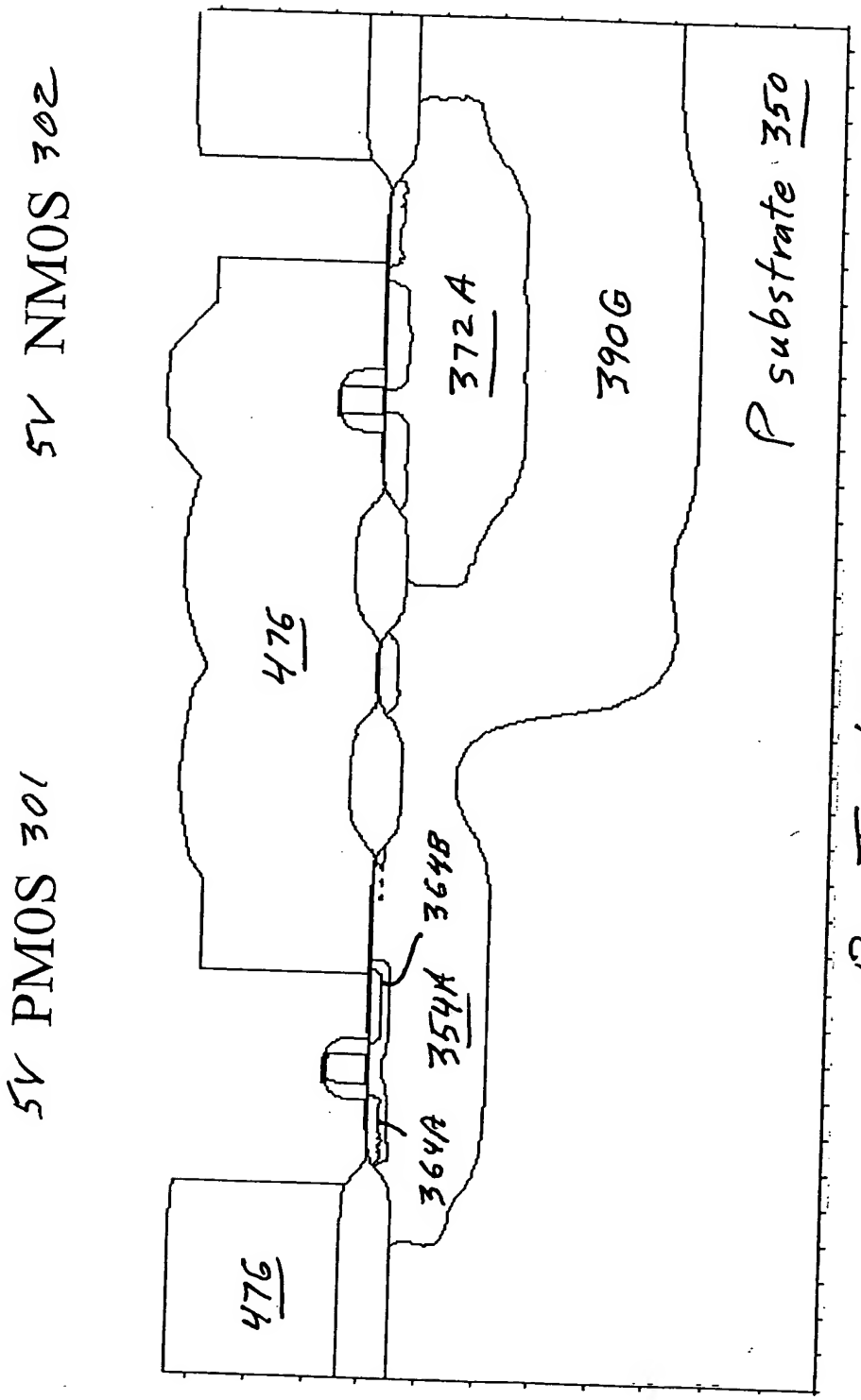
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Sidewall Spacers

Fig. 61E



P+ Implant
Fig. 62A

High F_T Layout

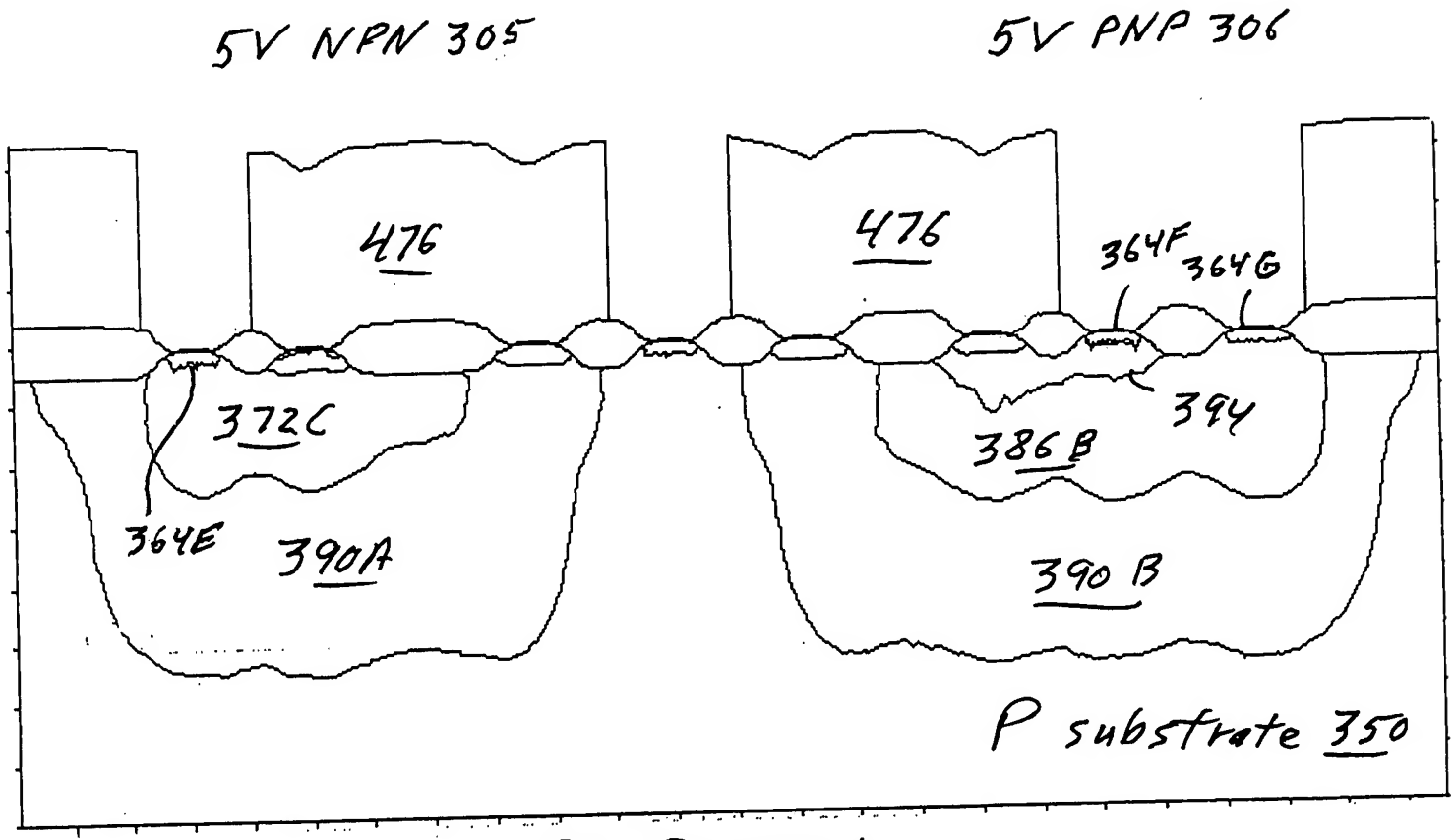


Fig. 62B

Conventional Layout

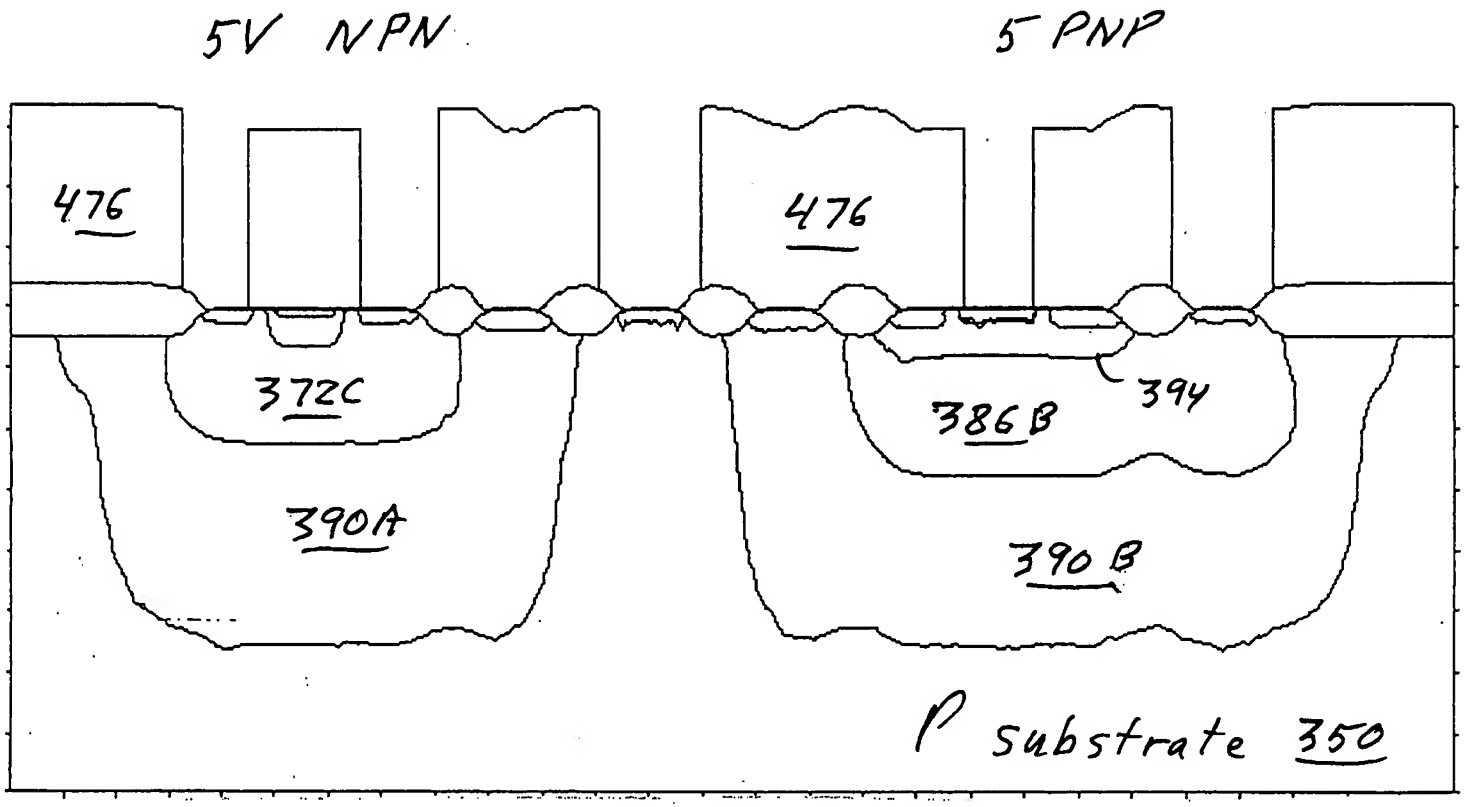


Fig. 62C

30V Lateral Trench DMOS 308

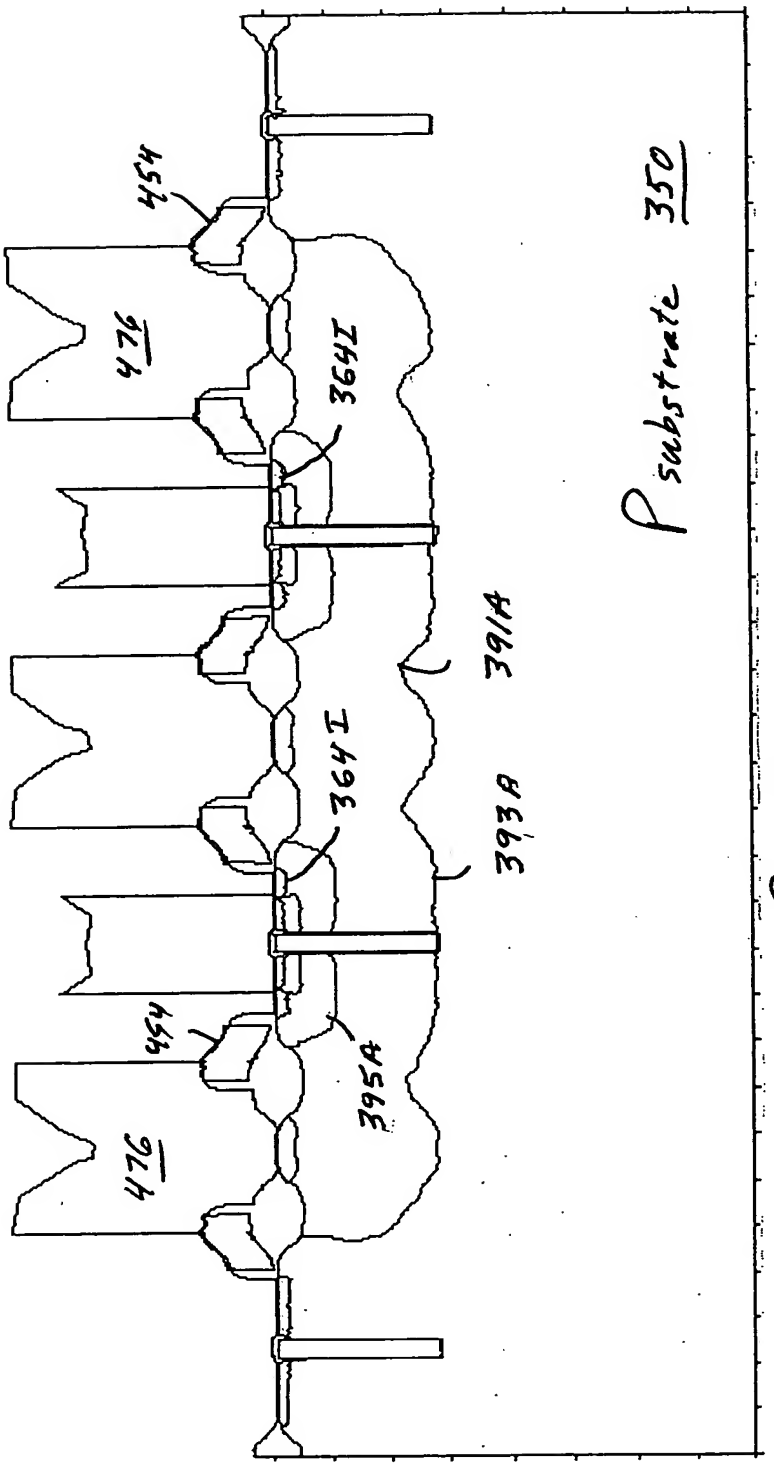
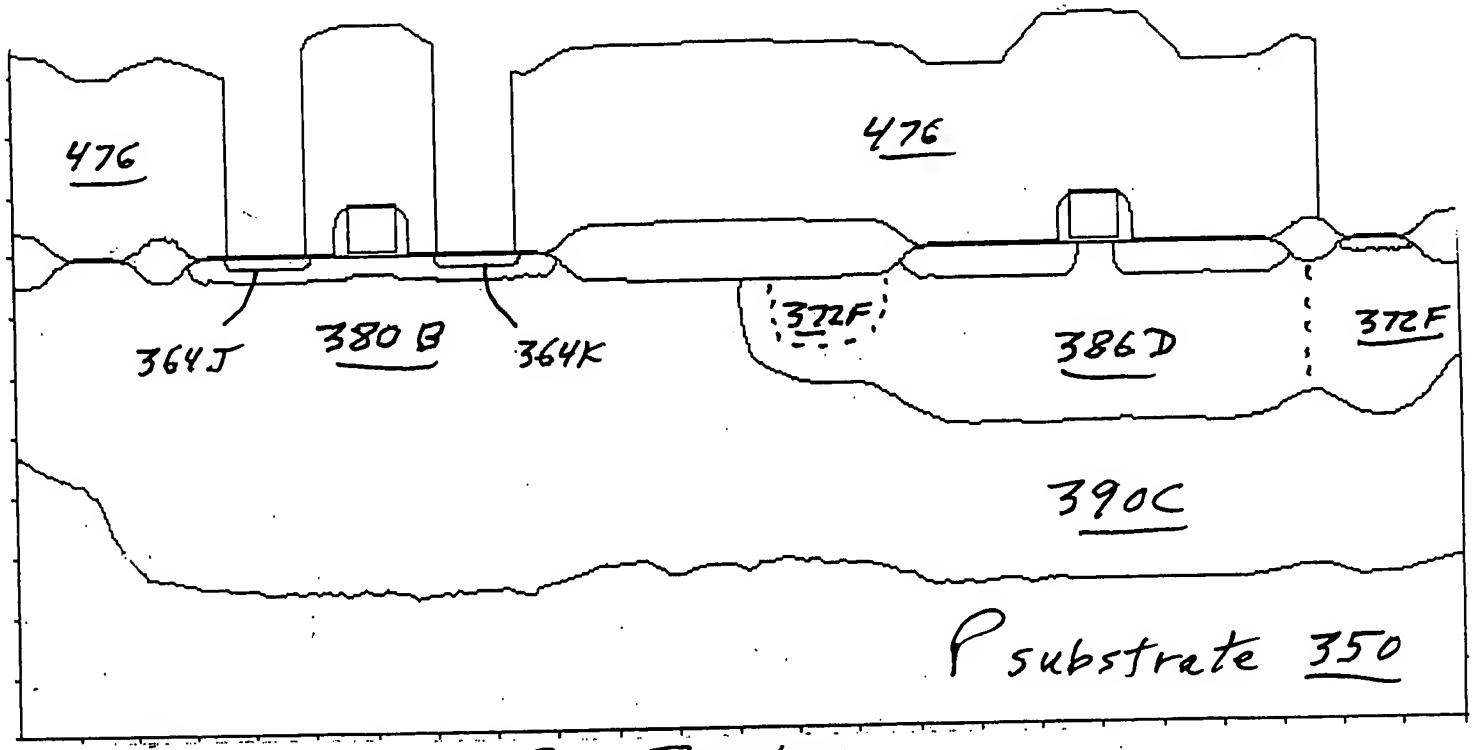


Fig. 62D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

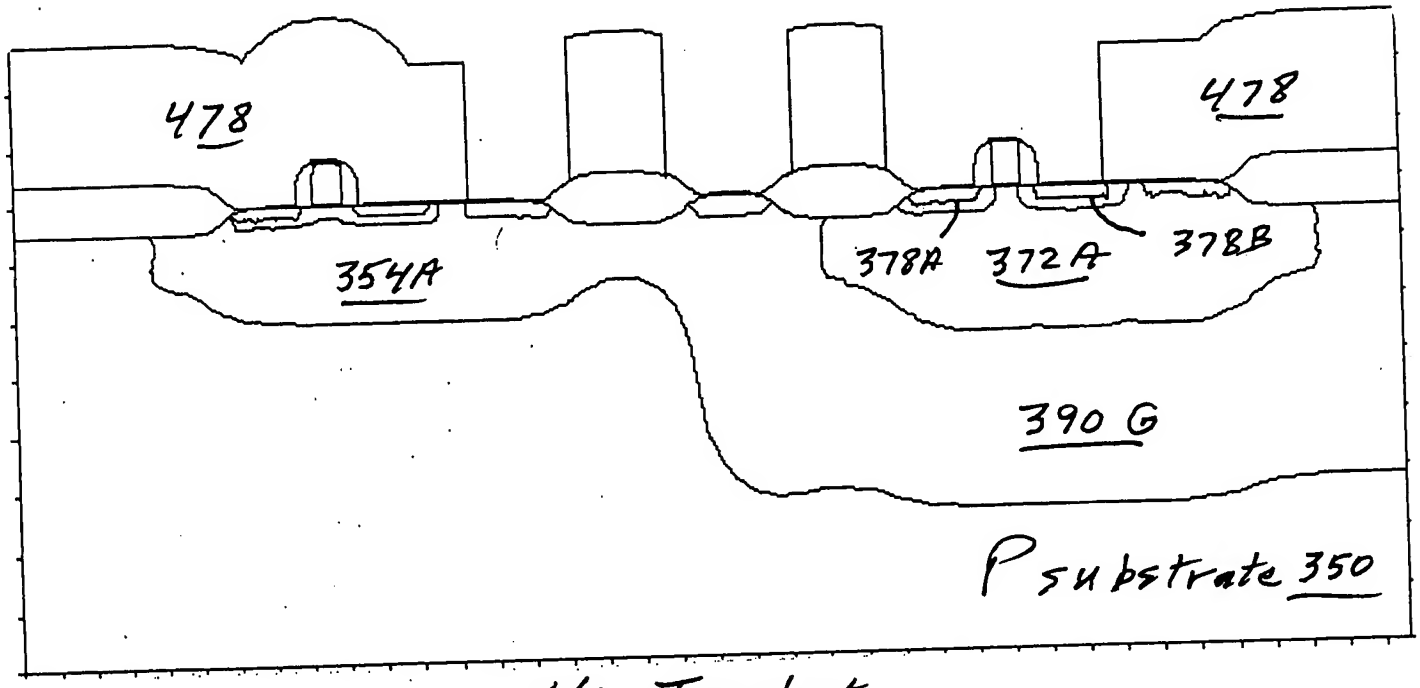


P+ Implant

Fig 62E

5V PMOS 301

5V NMOS 302



N+ Implant

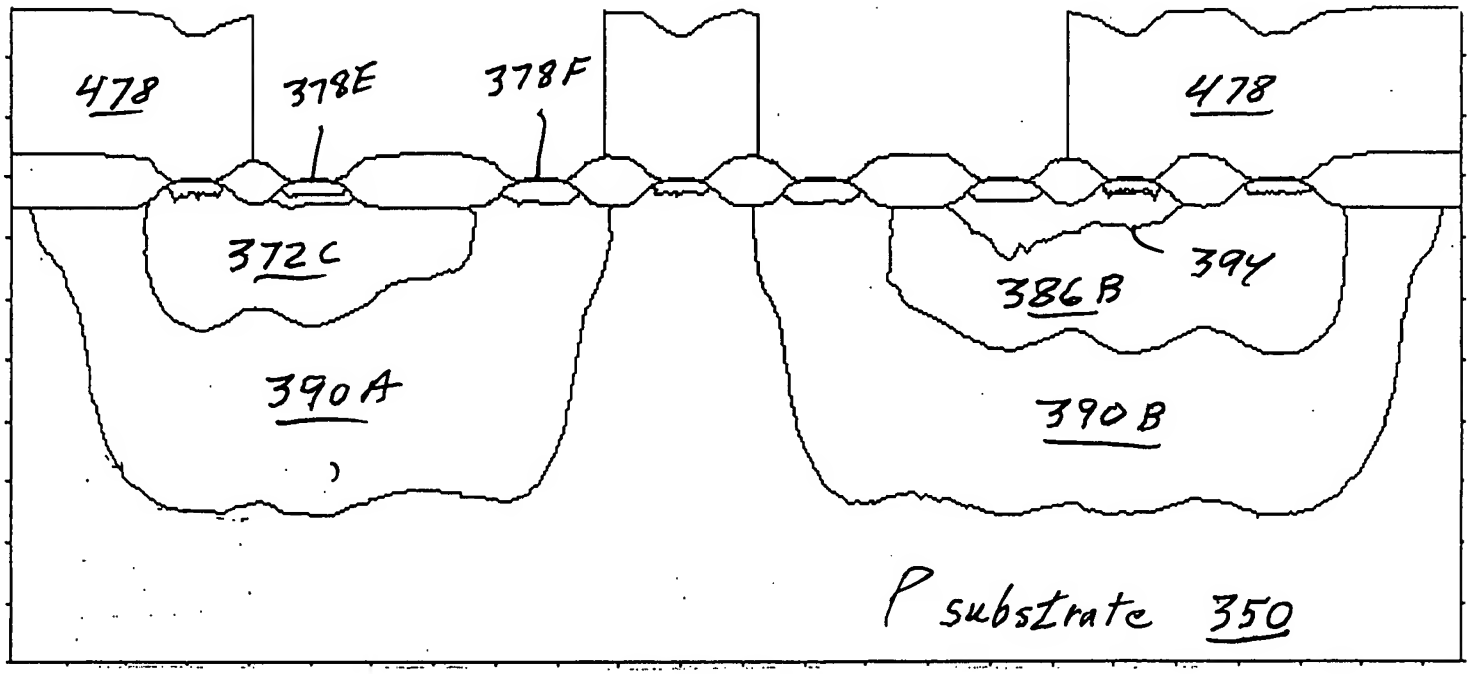
Fig. 63A

6/12/96

High F_T Layout

5V NPN 305

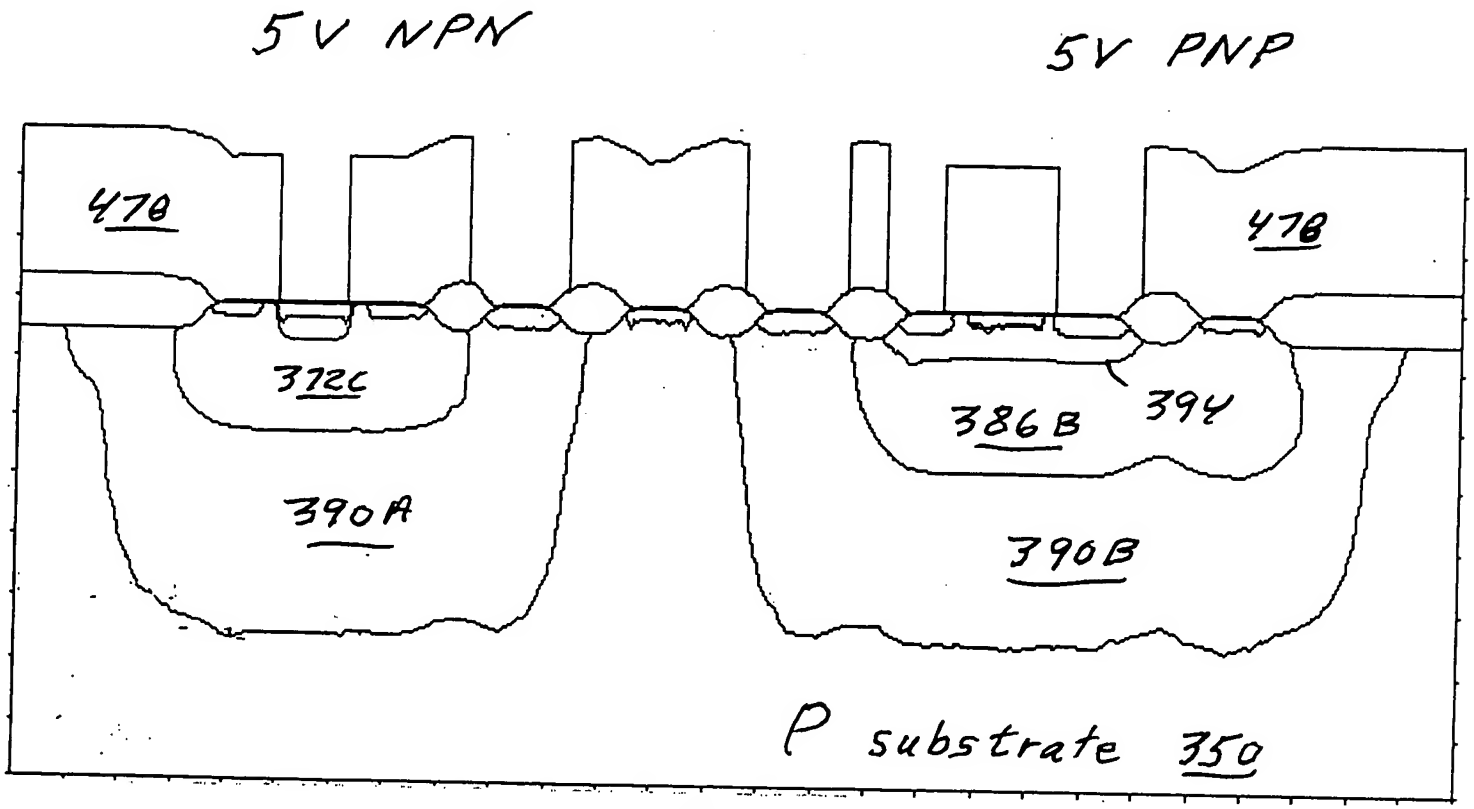
5V PNP 306



N+ Implant

Fig. 63B

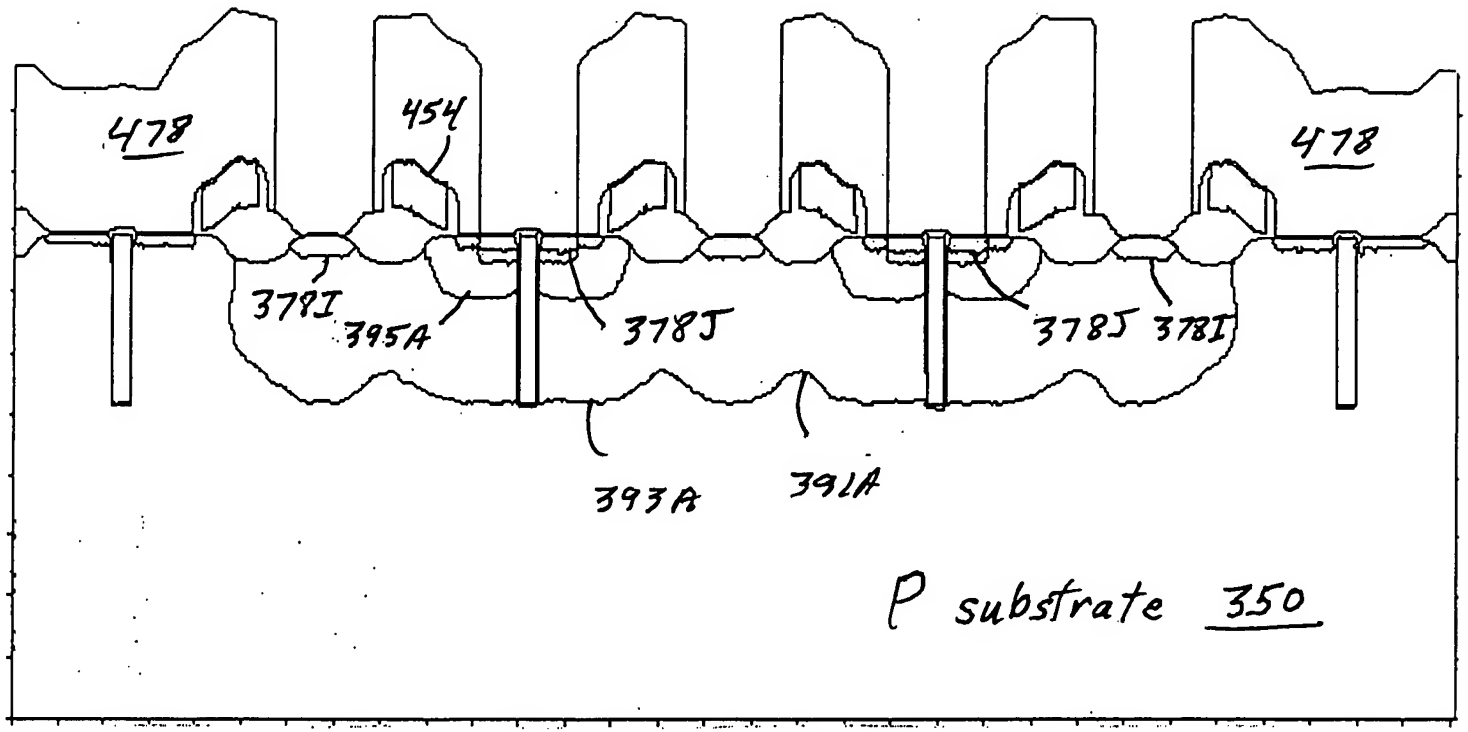
Conventional Layout



Nt Implant

Fig. 63C

30V Lateral Trench DMOS 308

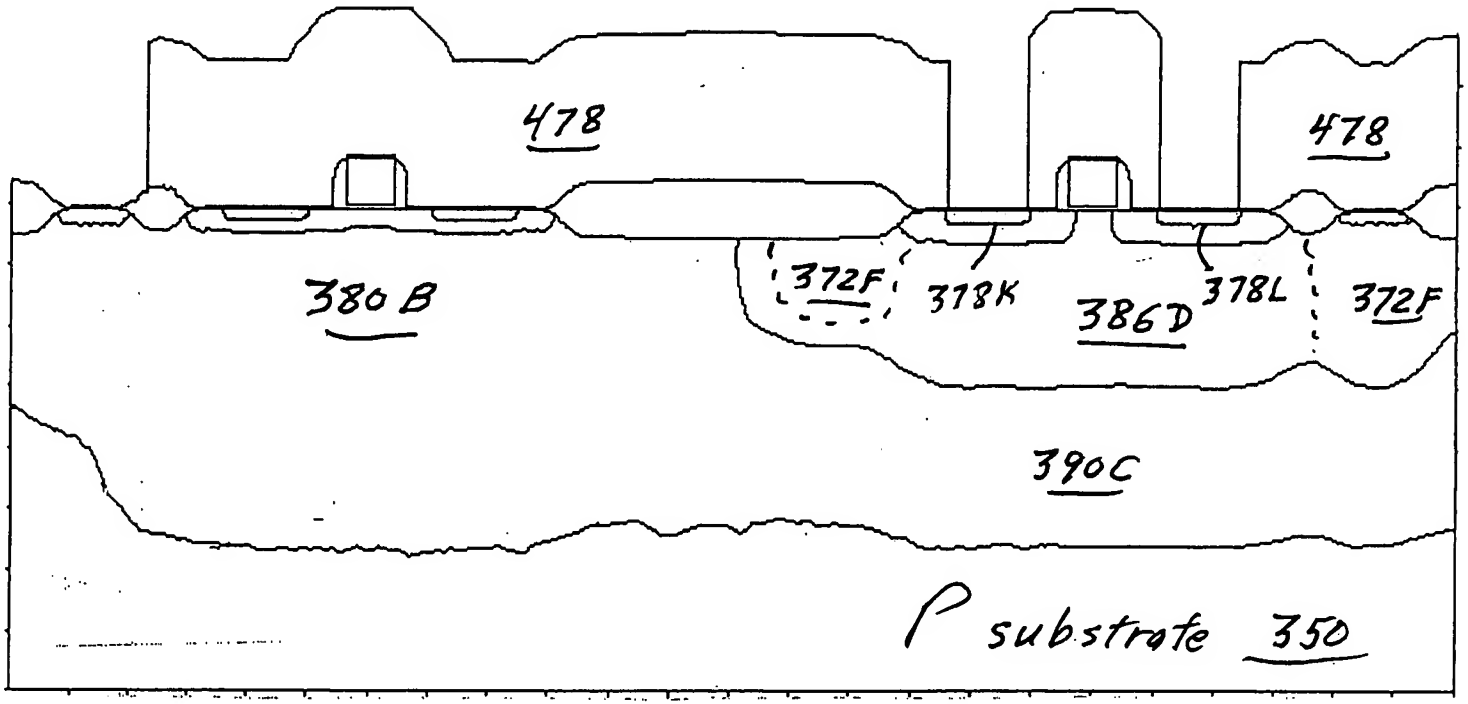


N+ Implant

Fig 63D

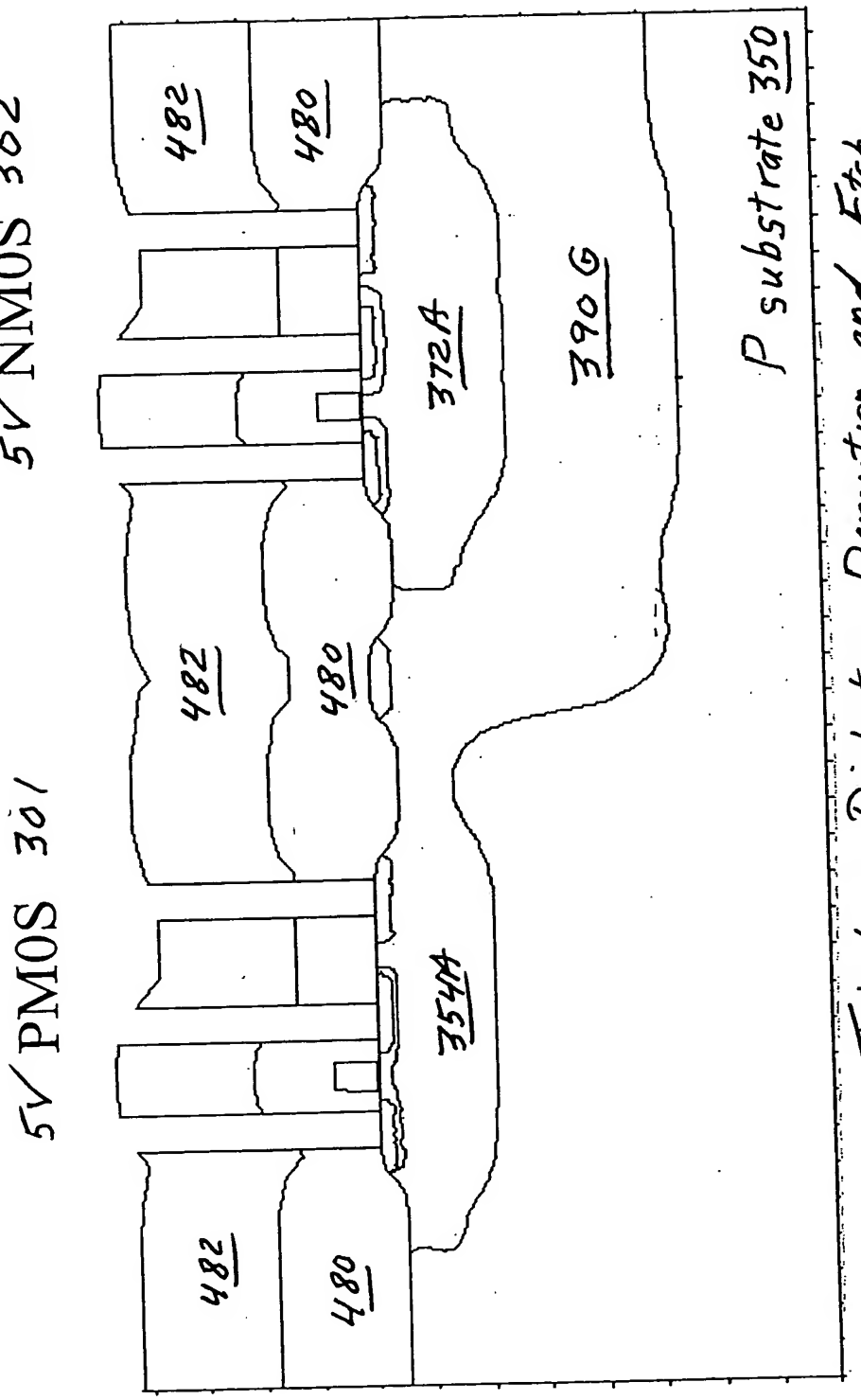
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



N+ Implant

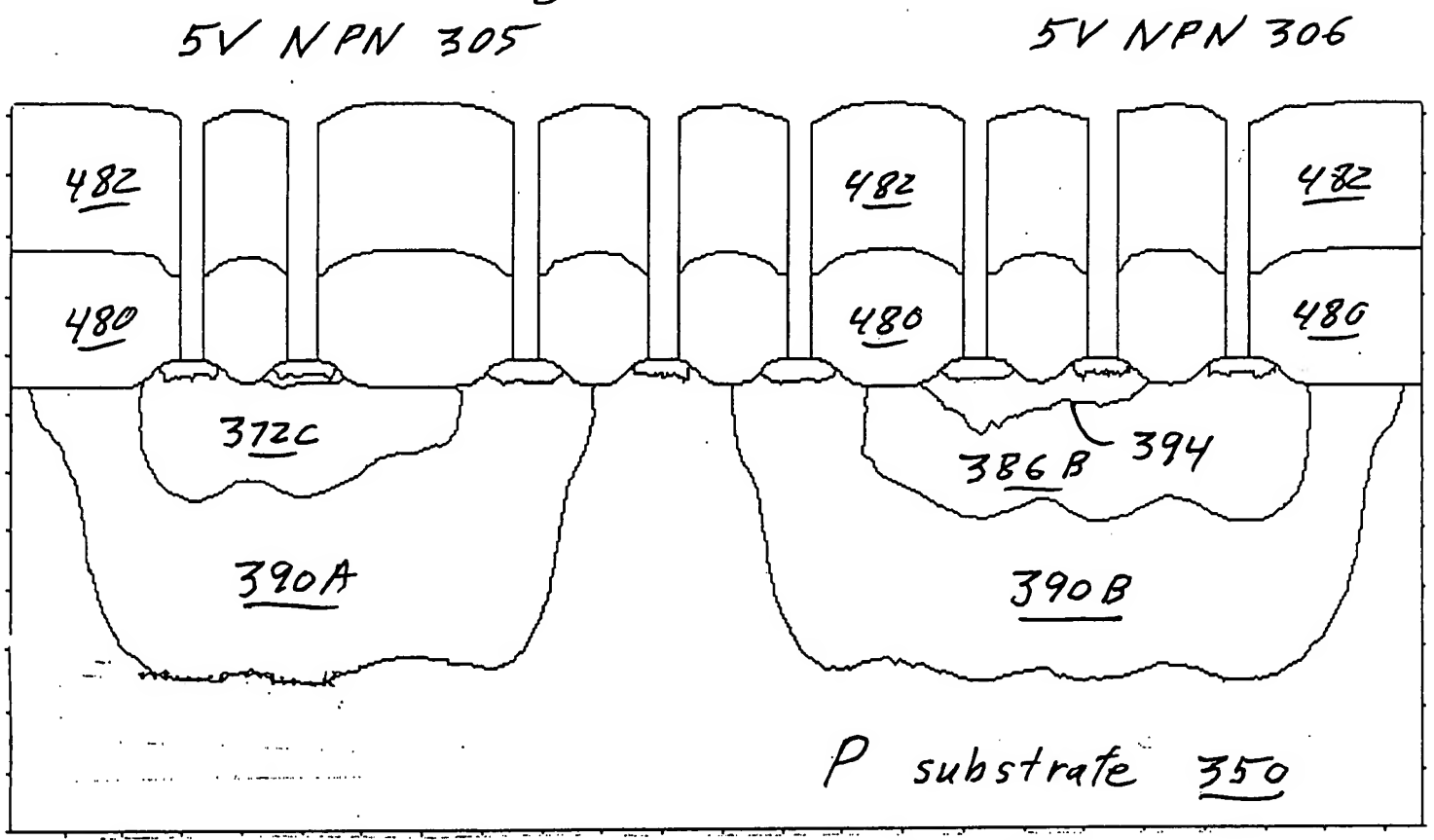
Fig 63E



Interlayer Dielectric Deposition and Etch

Fig. 6A

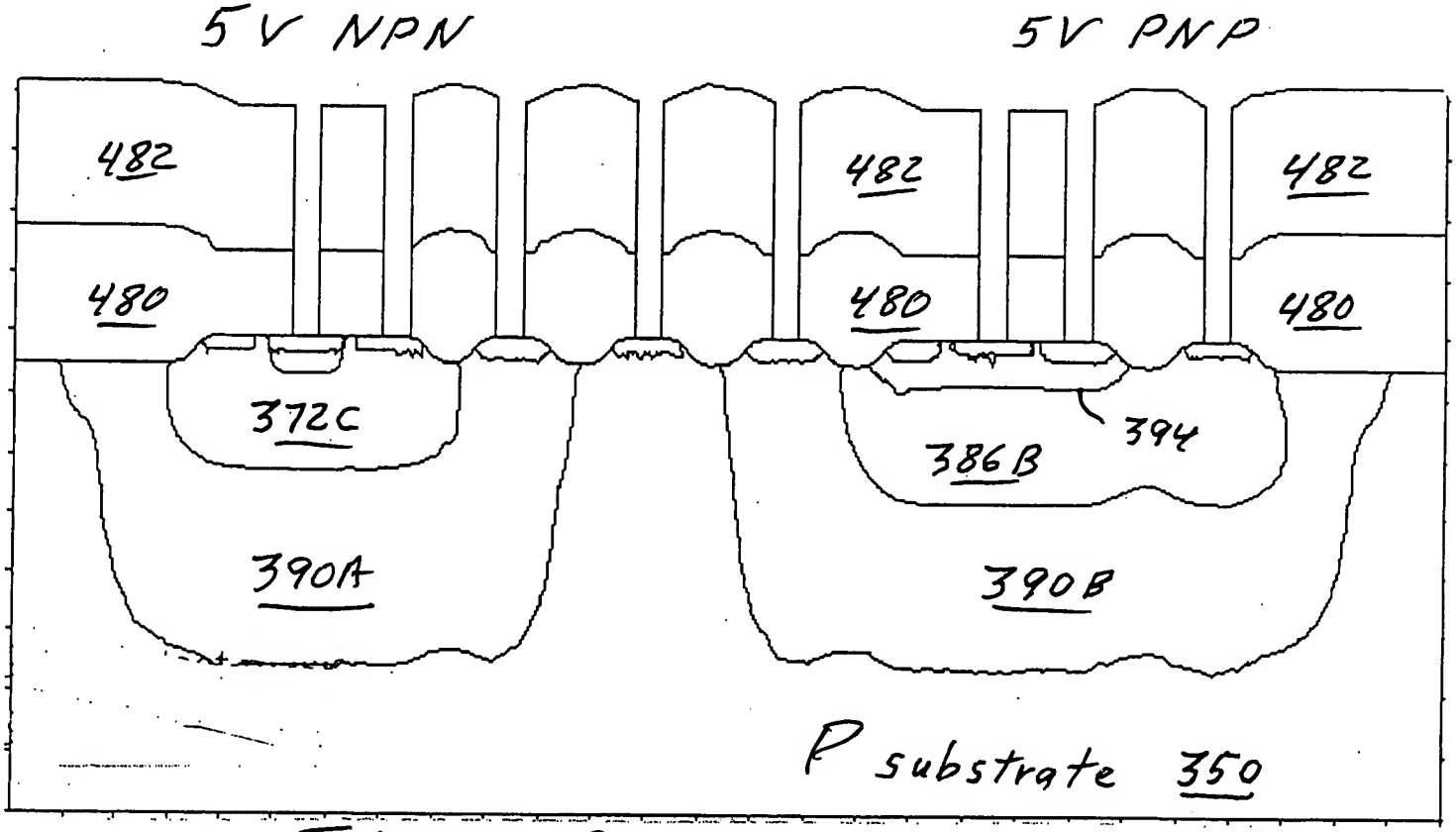
High F_T Layout



Interlayer Dielectric Deposition and Etch

Fig. 64B

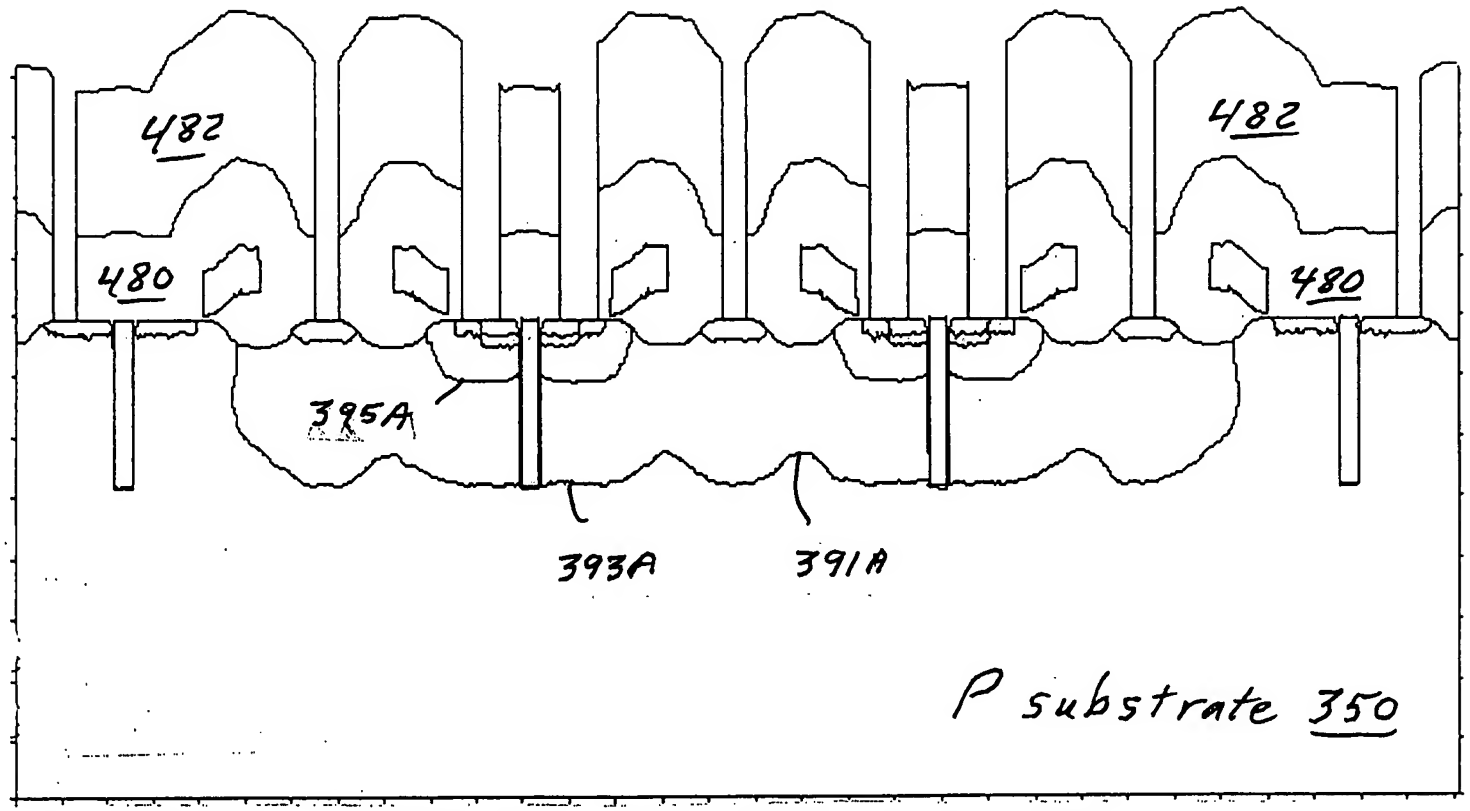
Conventional Layout



Interlayer Dielectric Deposition and Etch

Fig. 64C

30V Lateral Trench DMOS 308

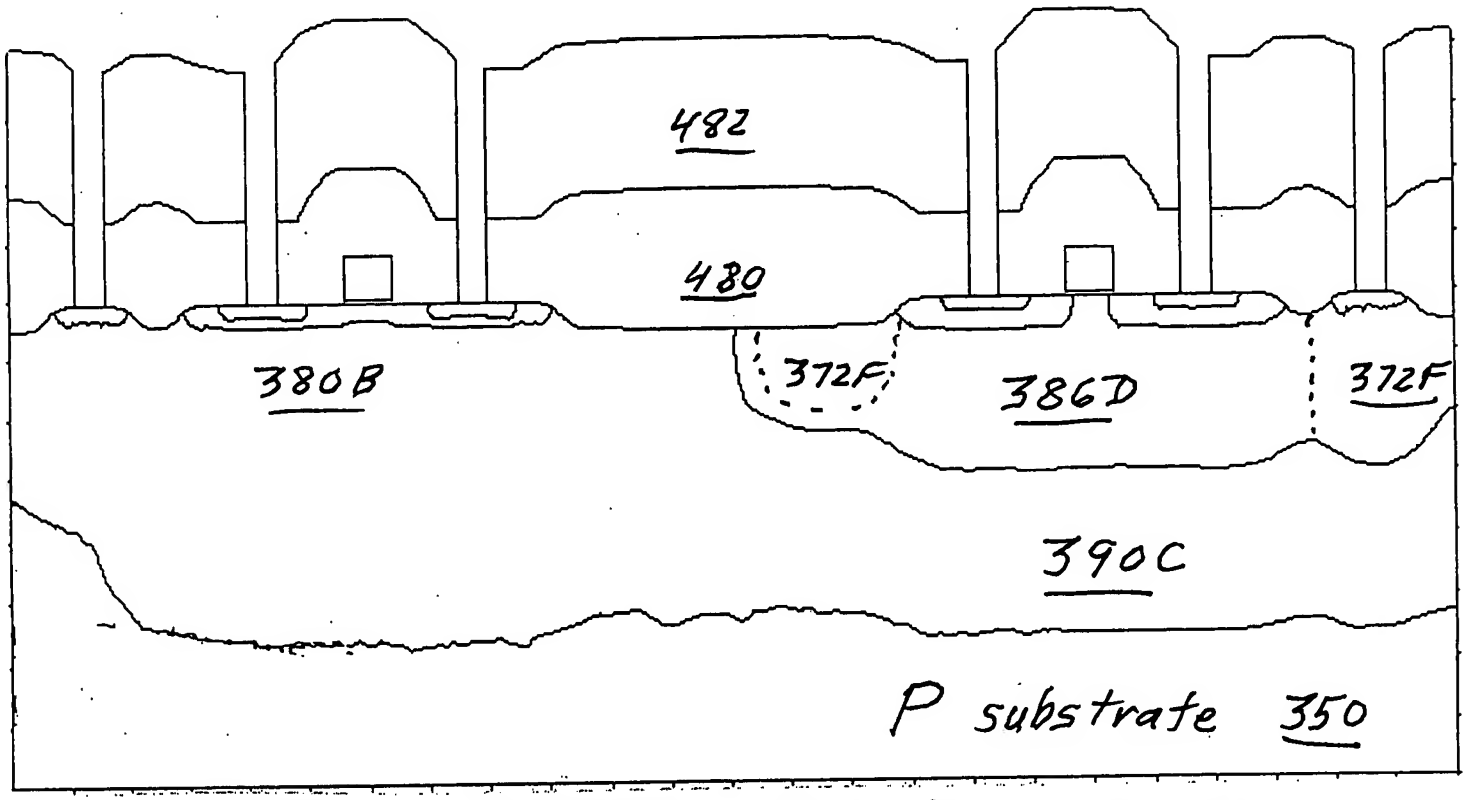


Interlayer Dielectric Deposition and Etch

Fig. 6D

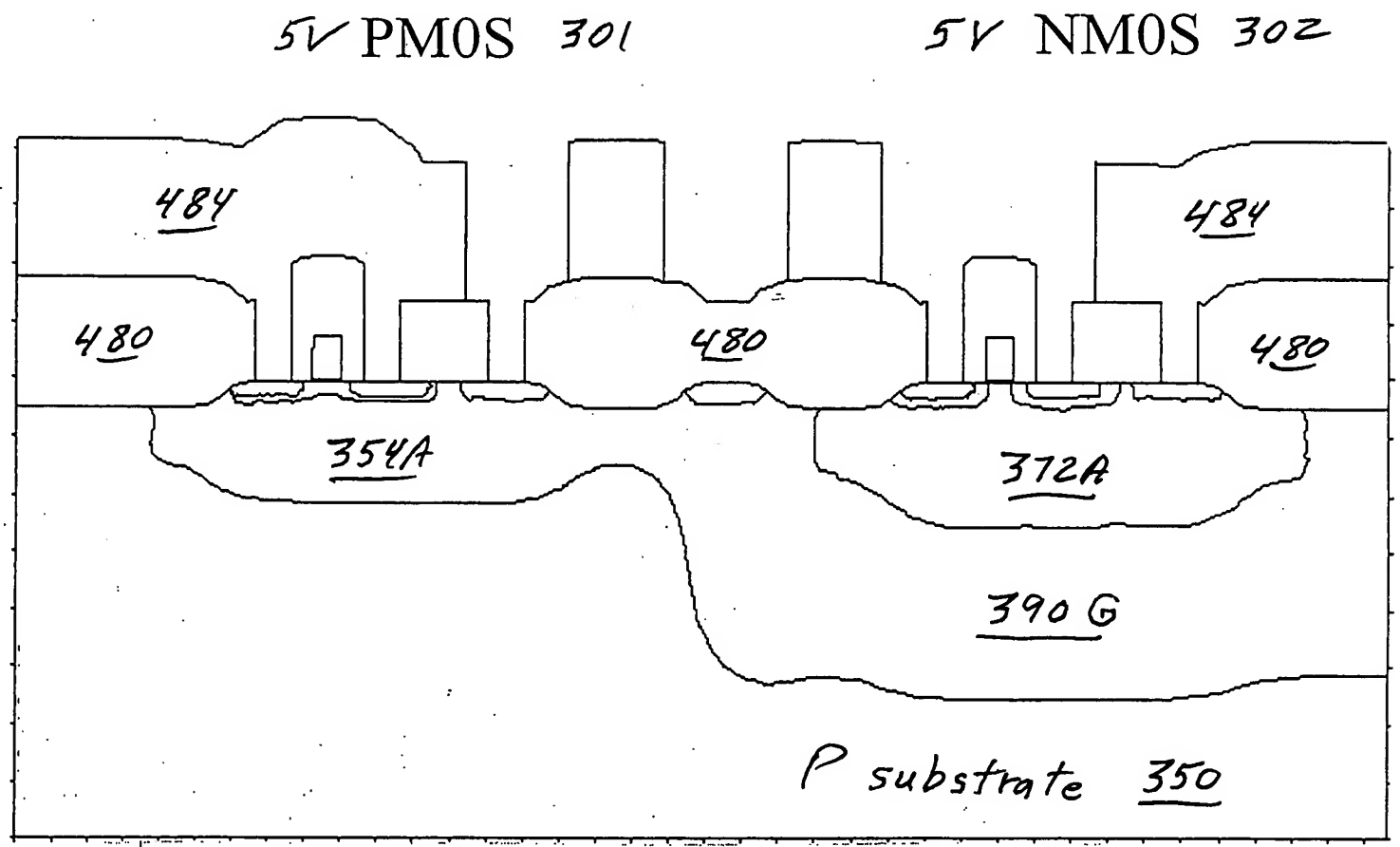
Symmetrical 12V CMOS

12V PM0S 309 12V NM0S 310



Interlayer Dielectric Deposition and Etch

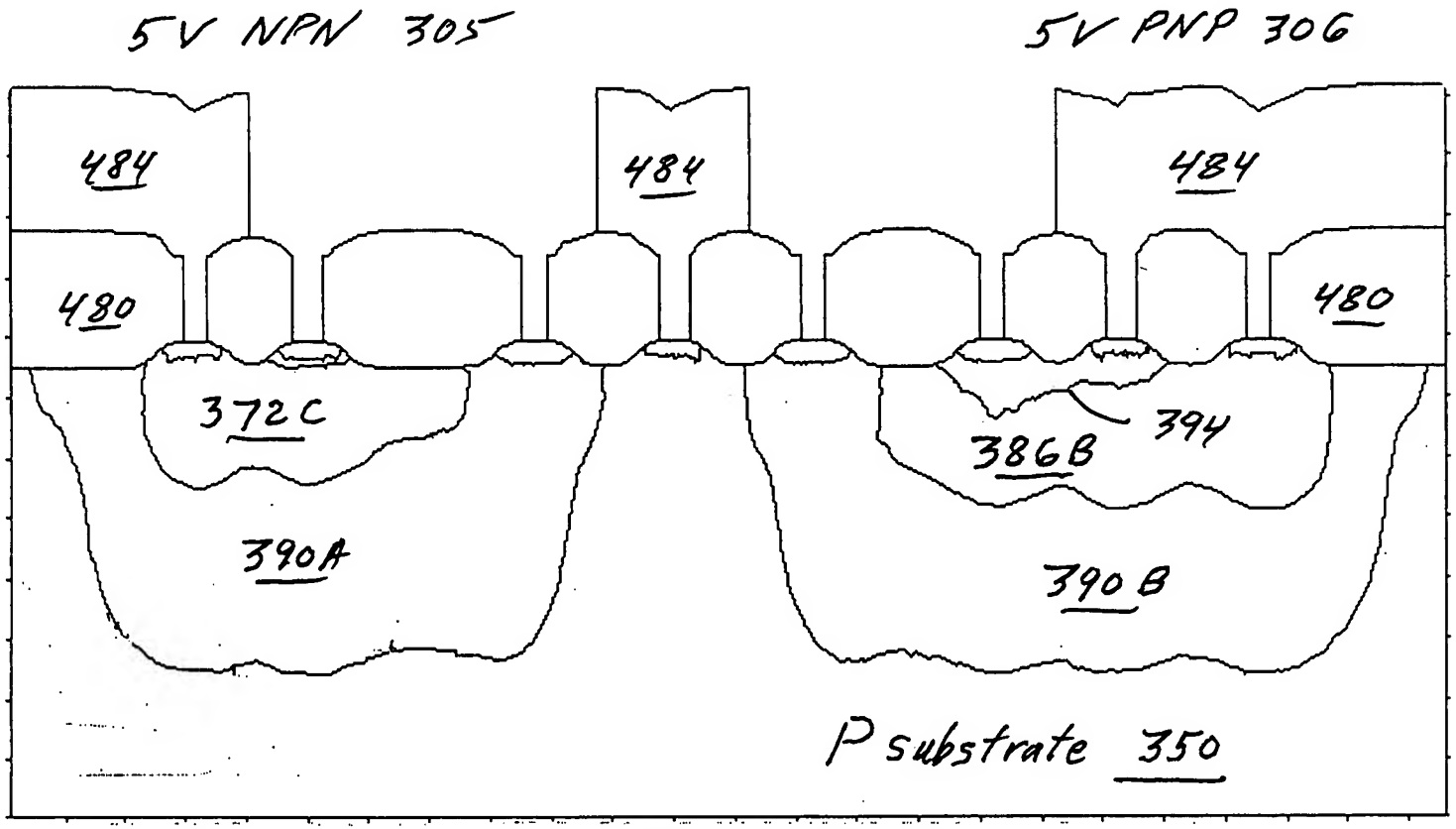
Fig 64E



N-plug Mask and Implant

Fig. 65A

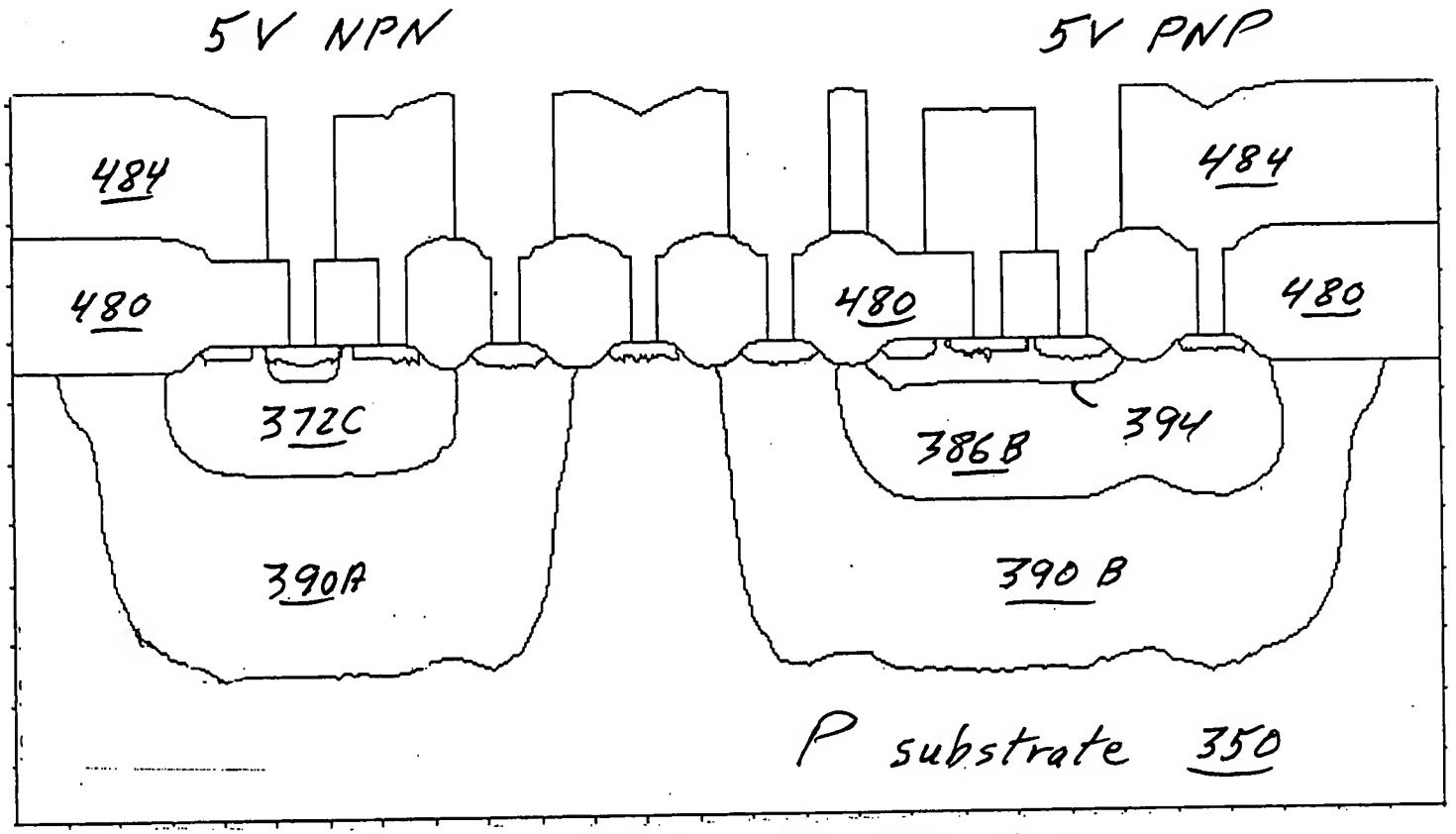
High F_T Layout



N-plug Mask and Implant

Fig 6-5B

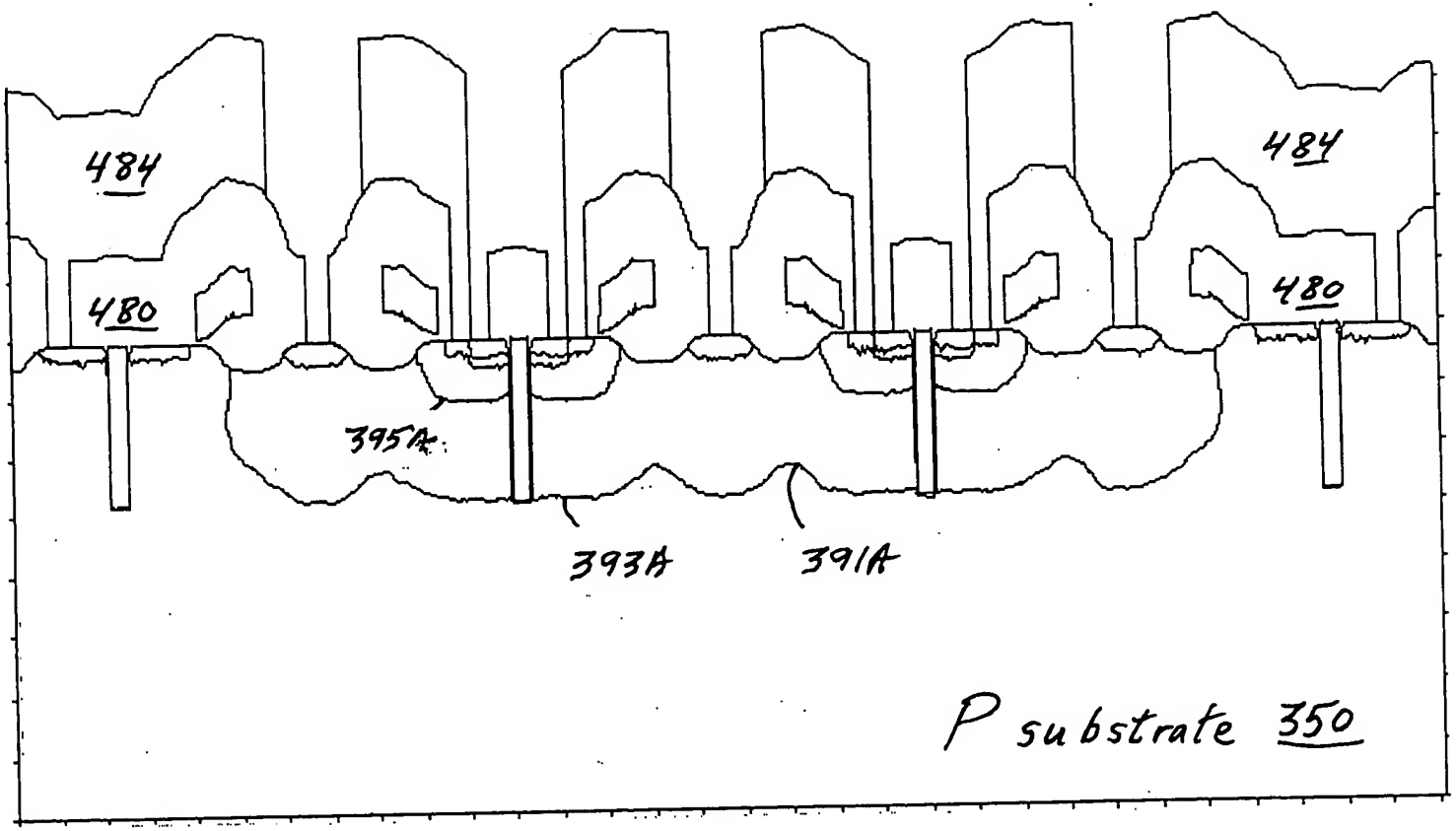
Conventional Layout



N-plug Mask and Implant

Fig. 6S C

30V Lateral Trench DMOS 308

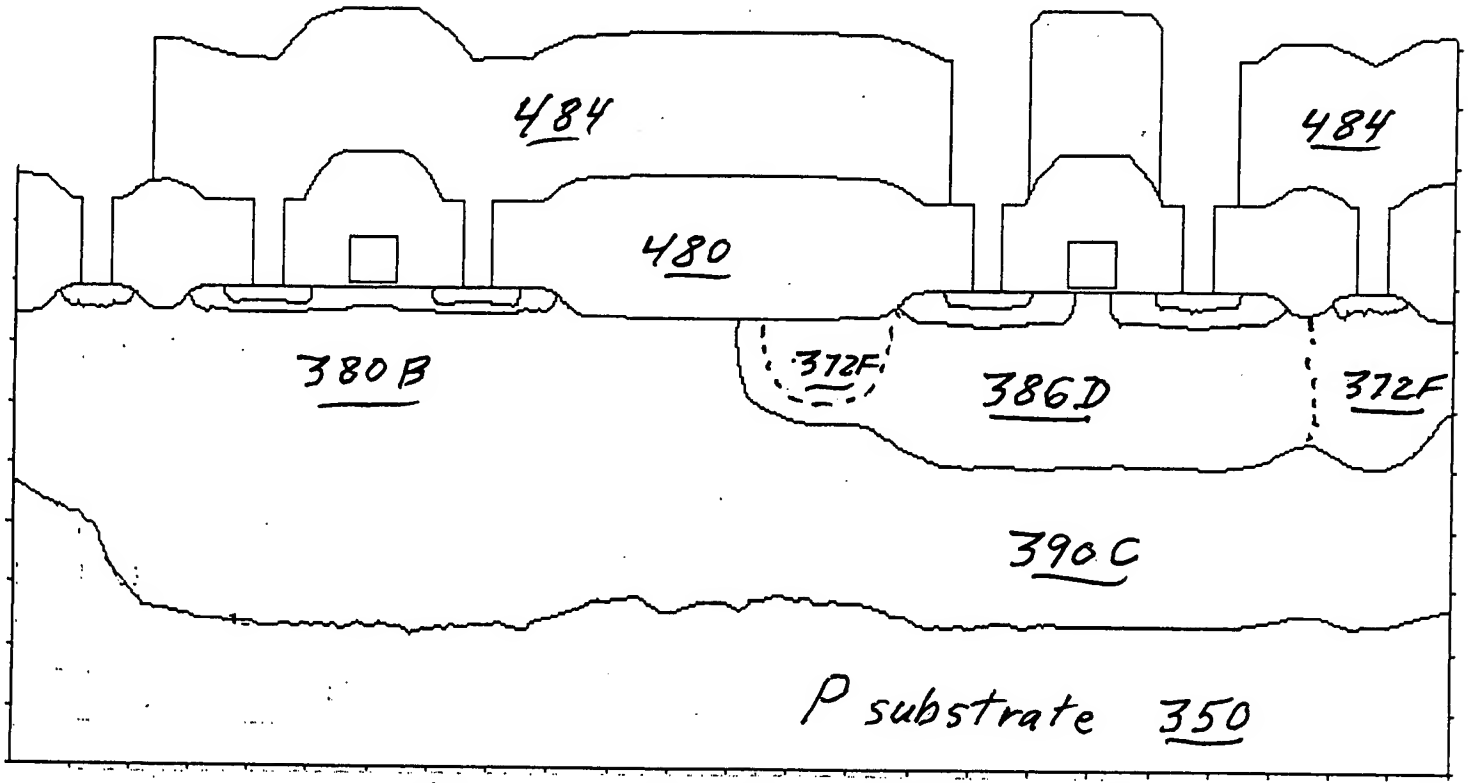


N-plug Mask and Implant

Fig 65D

Symmetrical 12V CMOS

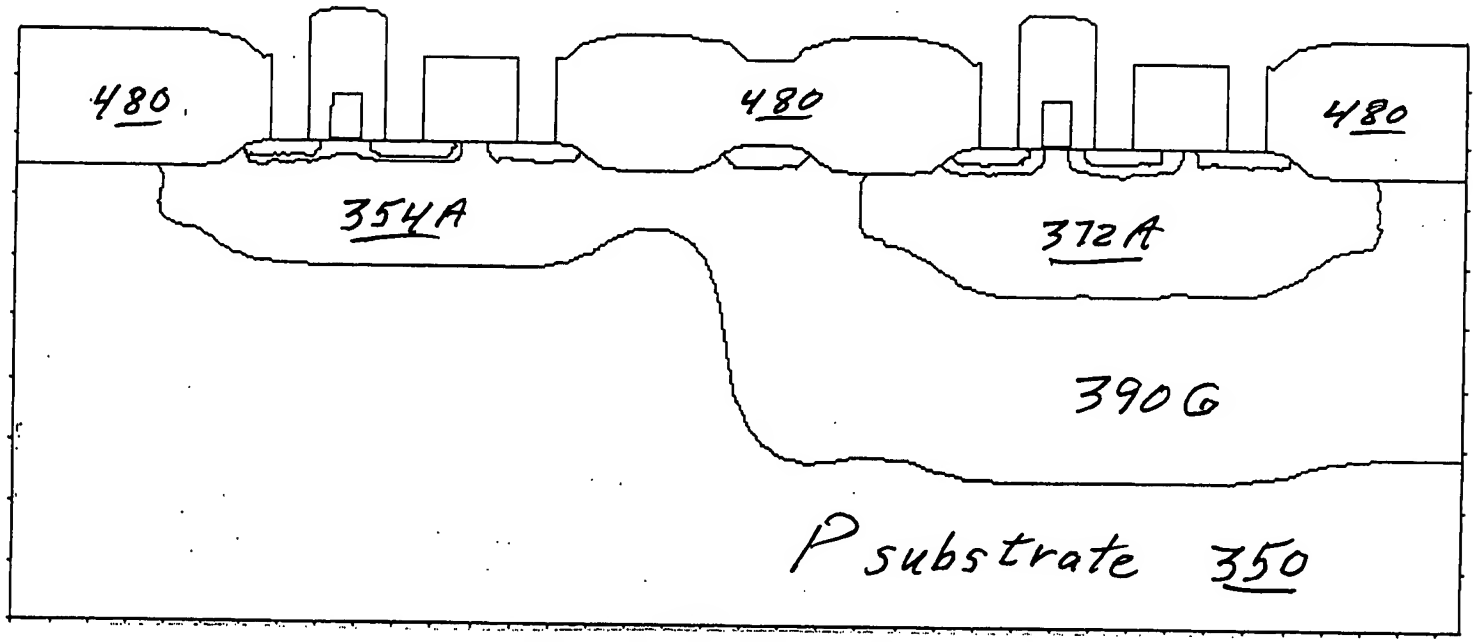
12V PMOS 309 12V NMOS 310



N-plug Mask and Implant

Fig 6 5E

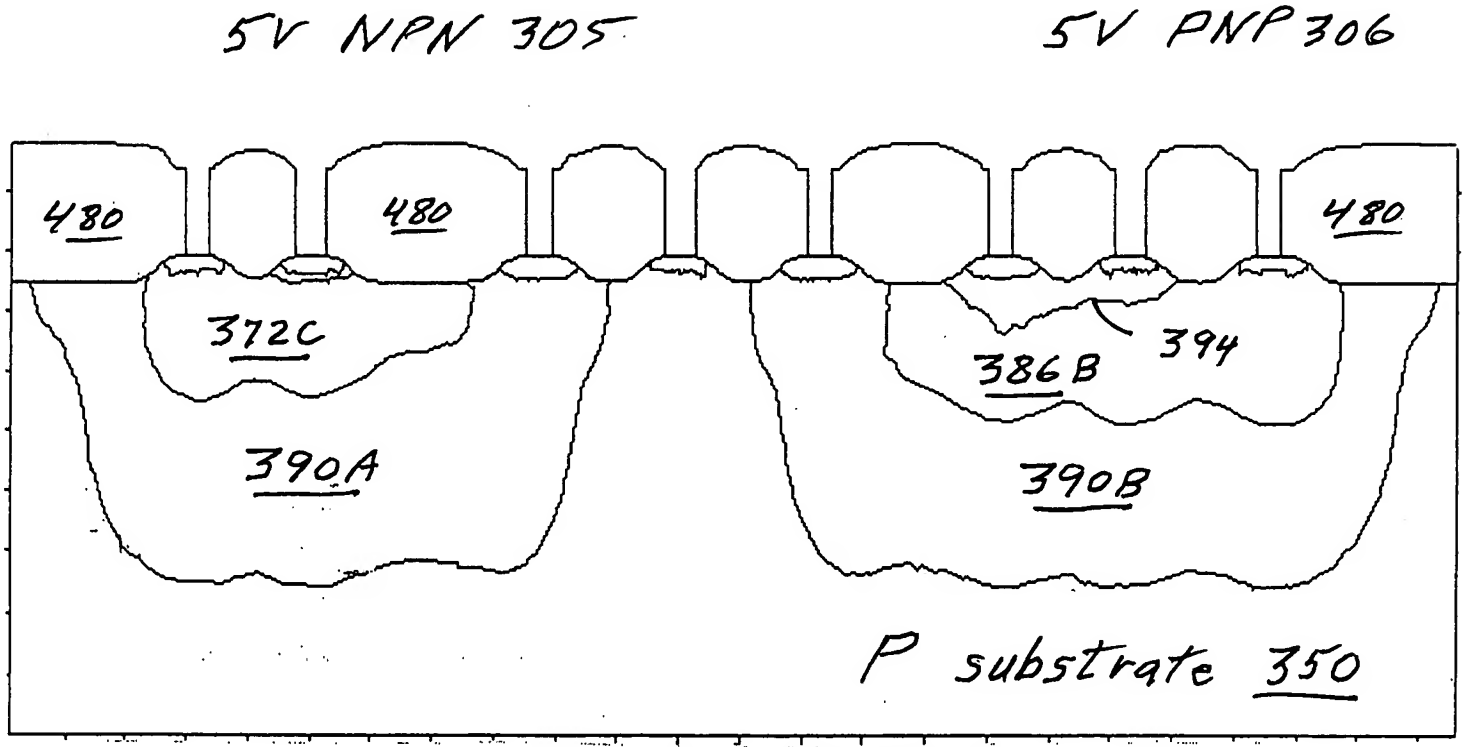
5V PMOS 301 5V NMOS 302



P-plug Implant

Fig. 66A

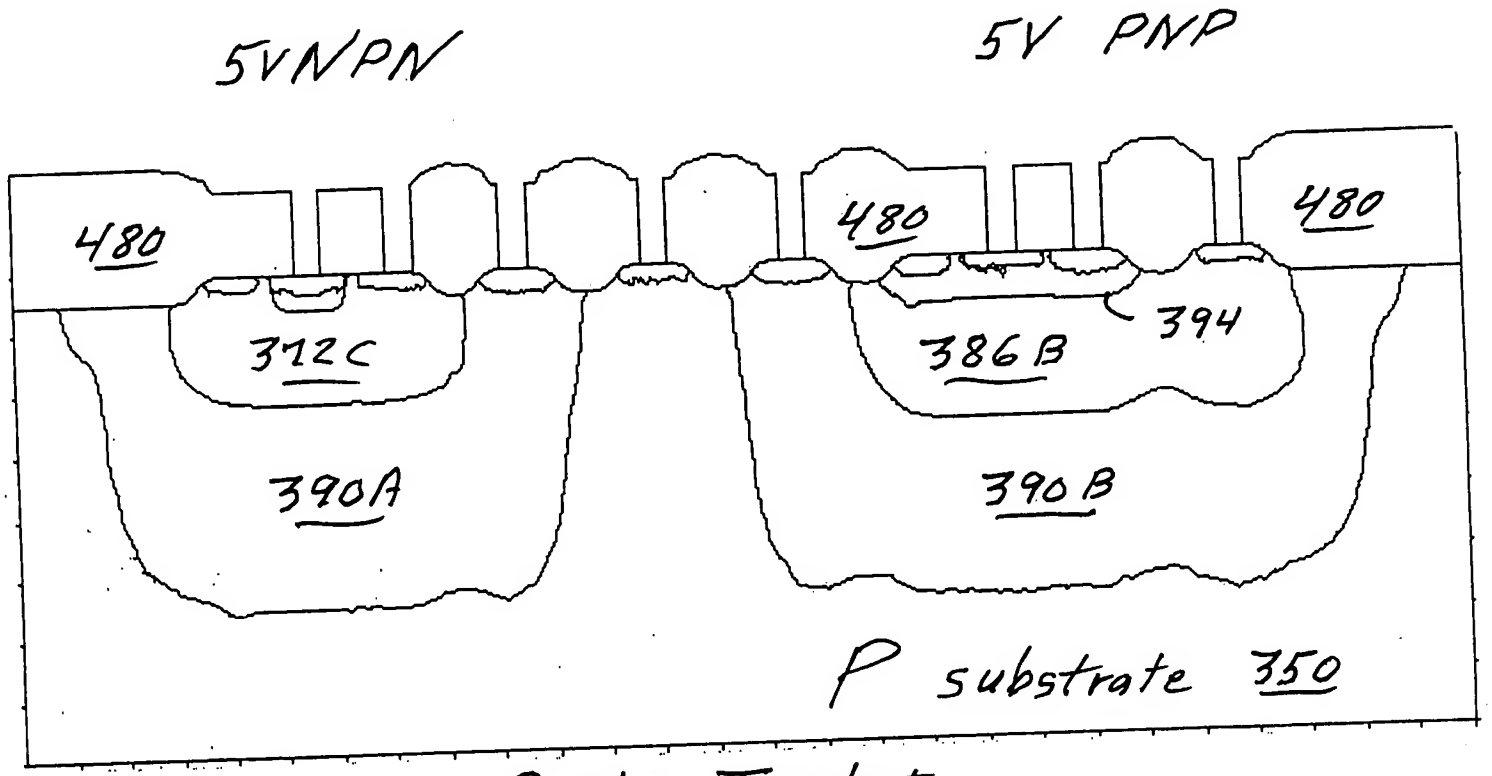
High F_T Layout



P-plug Implant

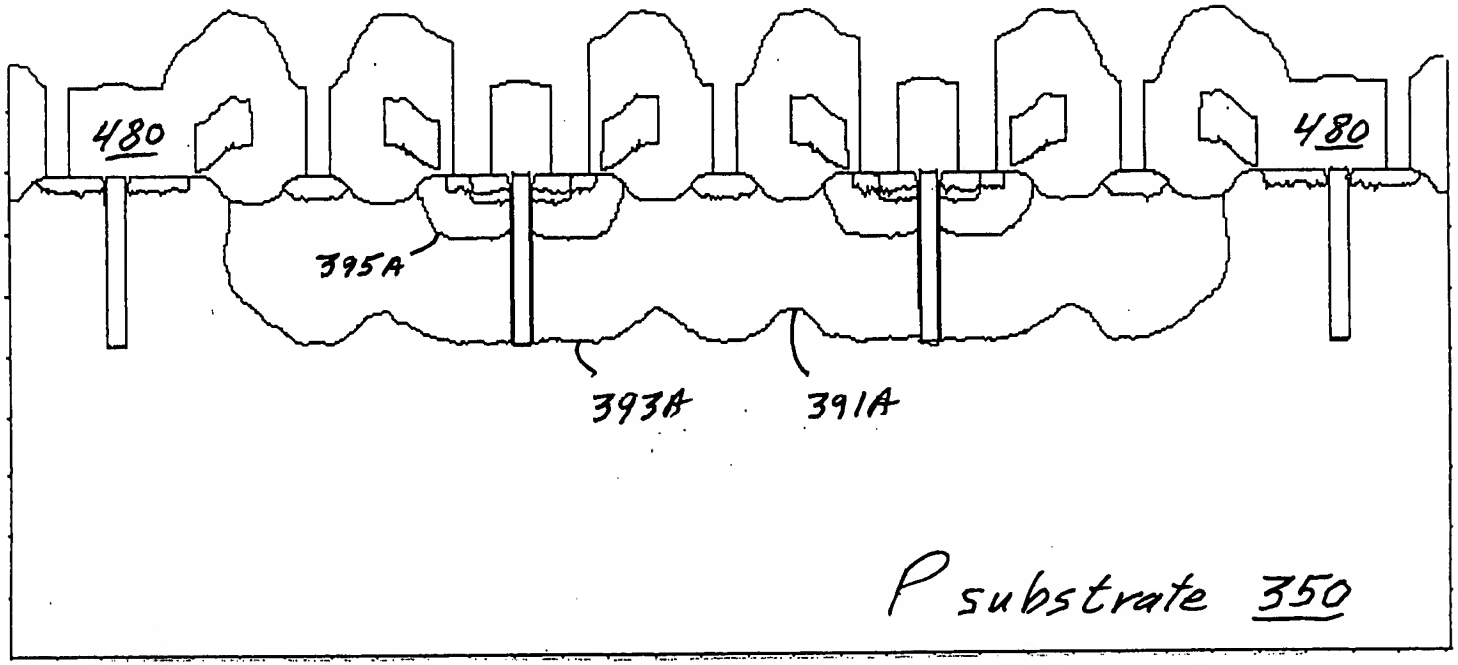
Fig. 66B

Conventional Layout



P-plug Implant
Fig. 66C

30V Lateral / Trench DMOS 308

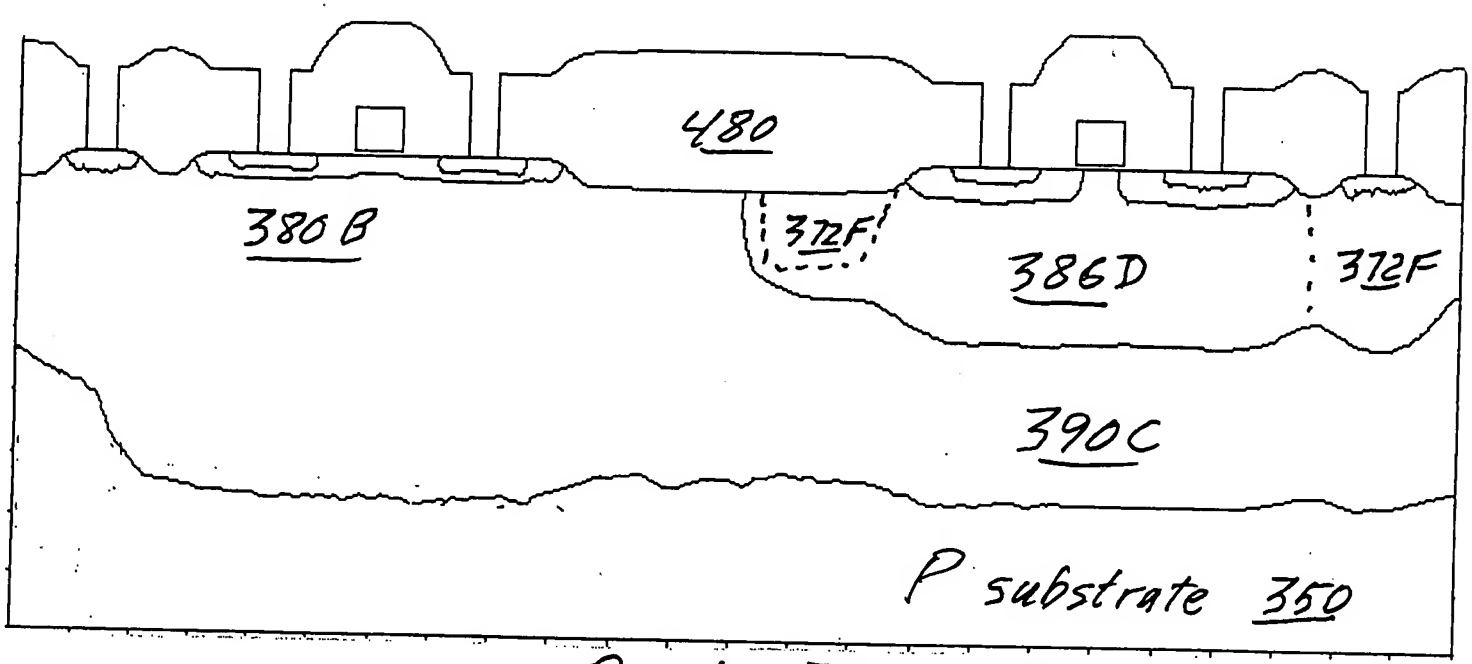


P-plug Implant

Fig. 66D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



P-plug Implant

Fig. 66E

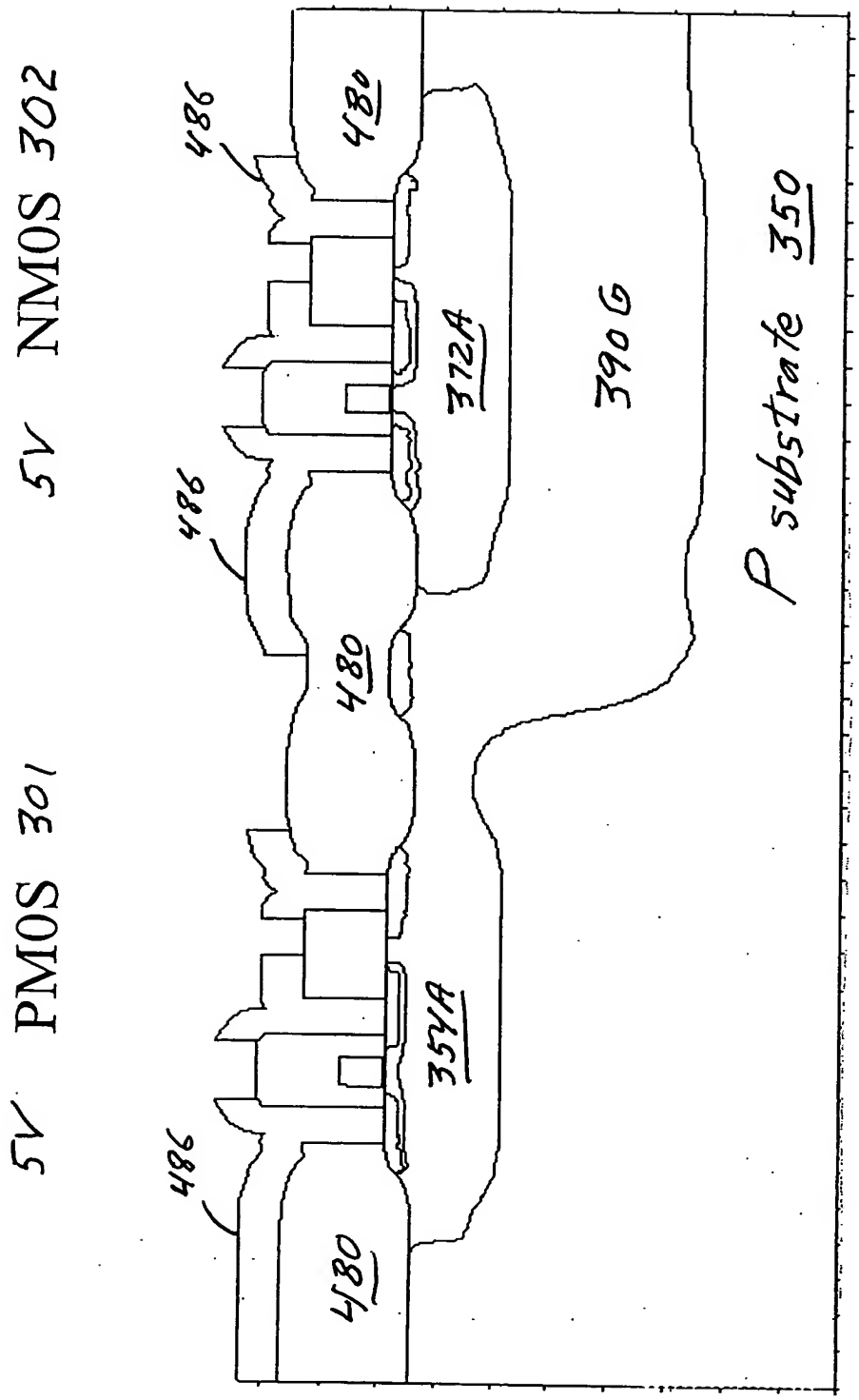

5V PMOS 301
5V NMOS 302
486
480
372A
390G
P substrate 350
3514
Metal Layer

Fig. 6A

High F_T Layout

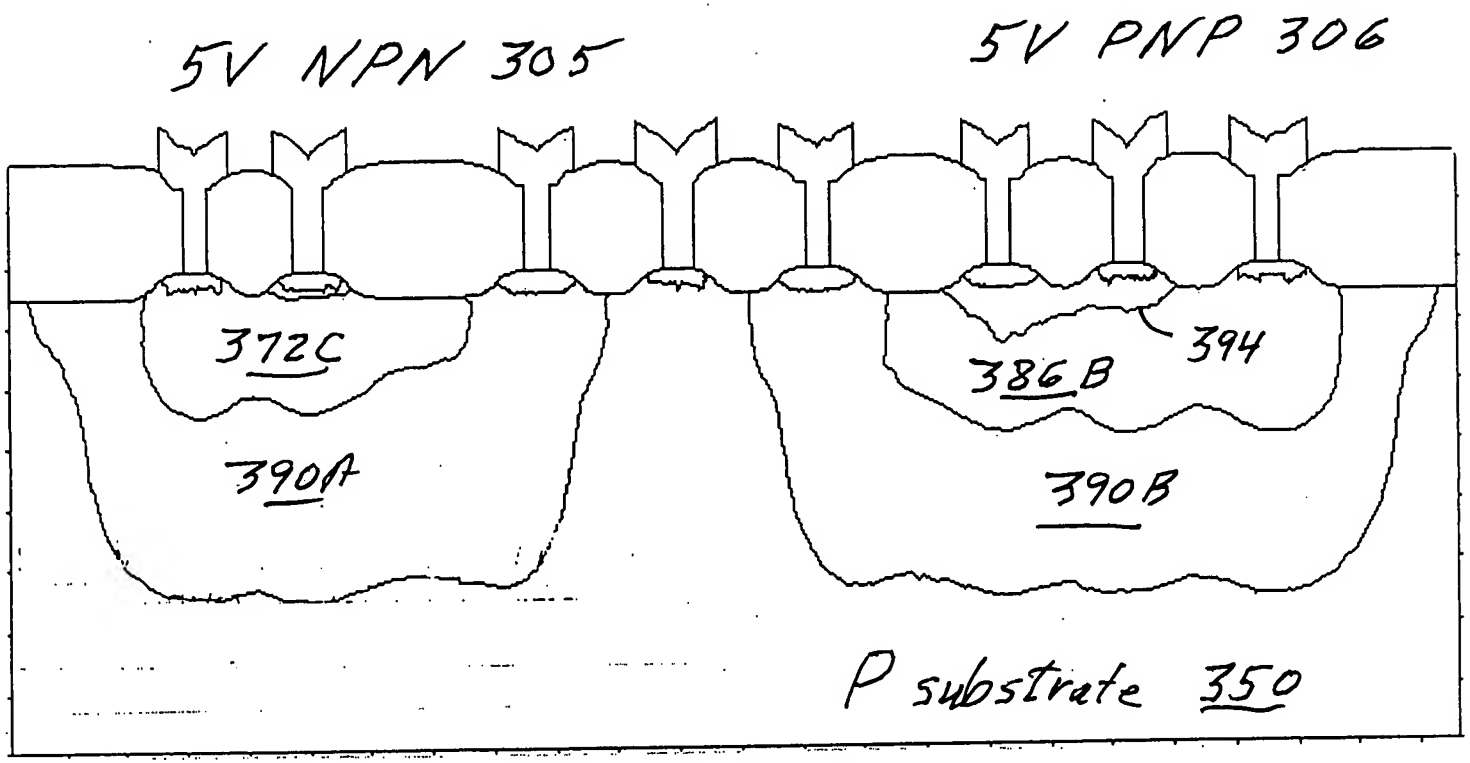
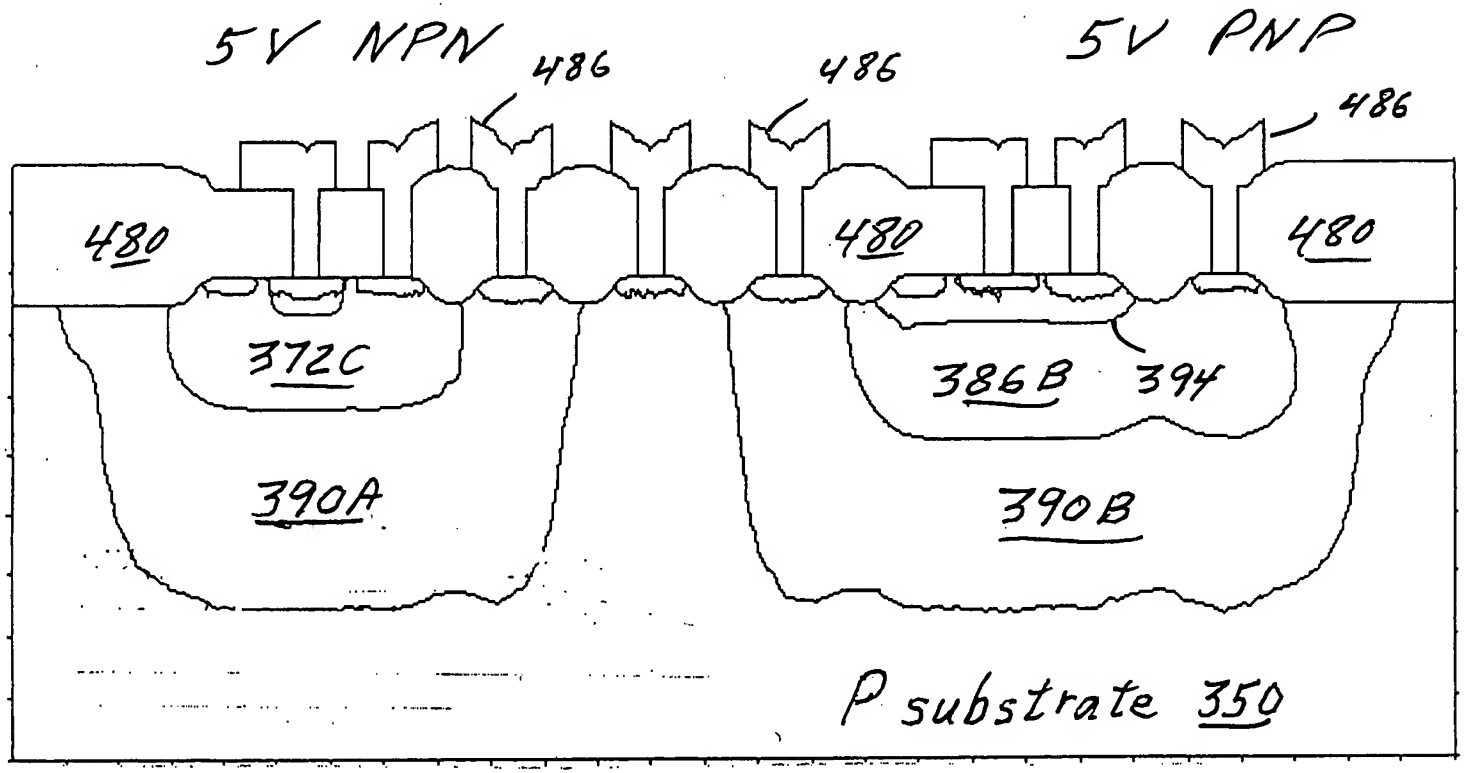


Fig. 67B

Conventional Layout



Metal Layer

Fig. 67C

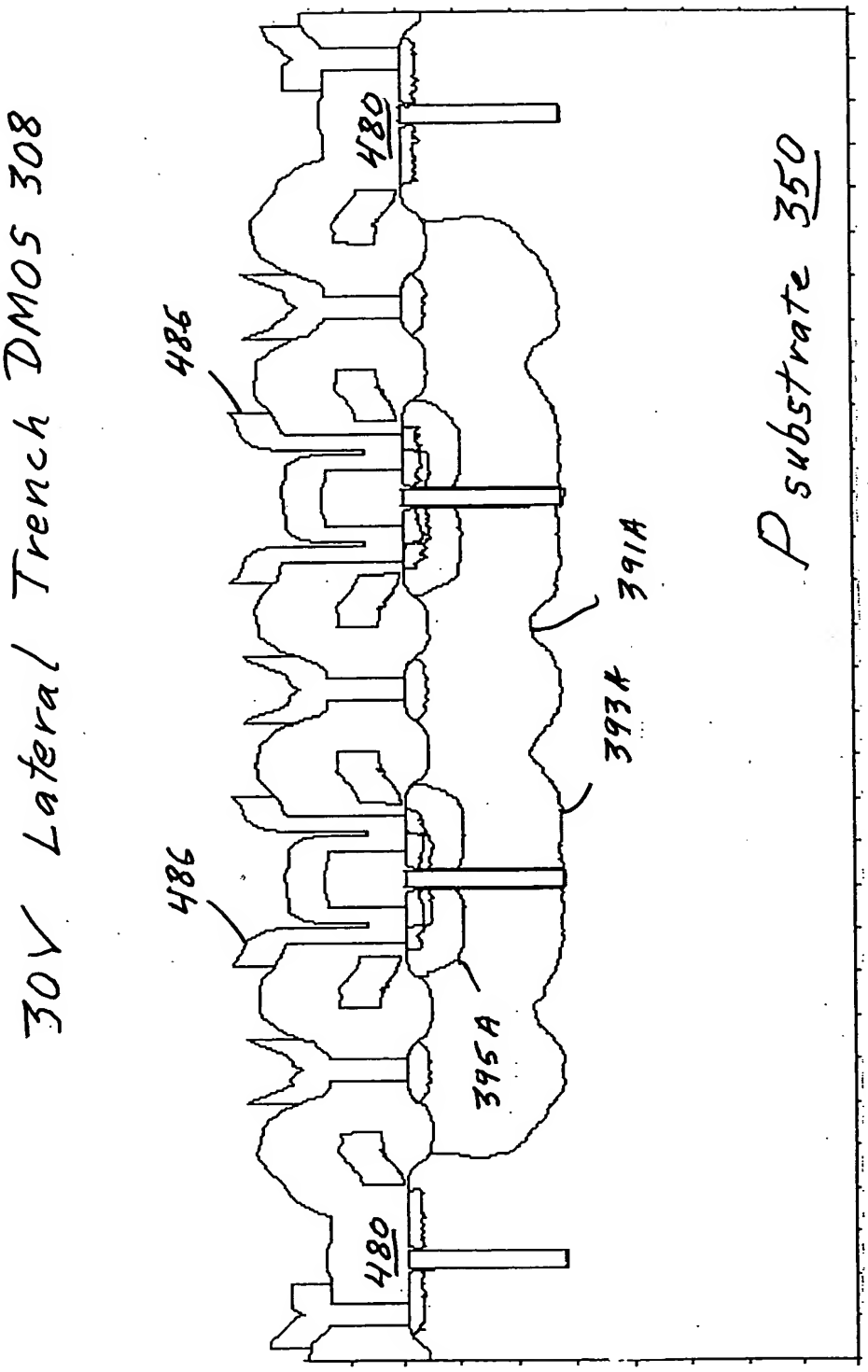
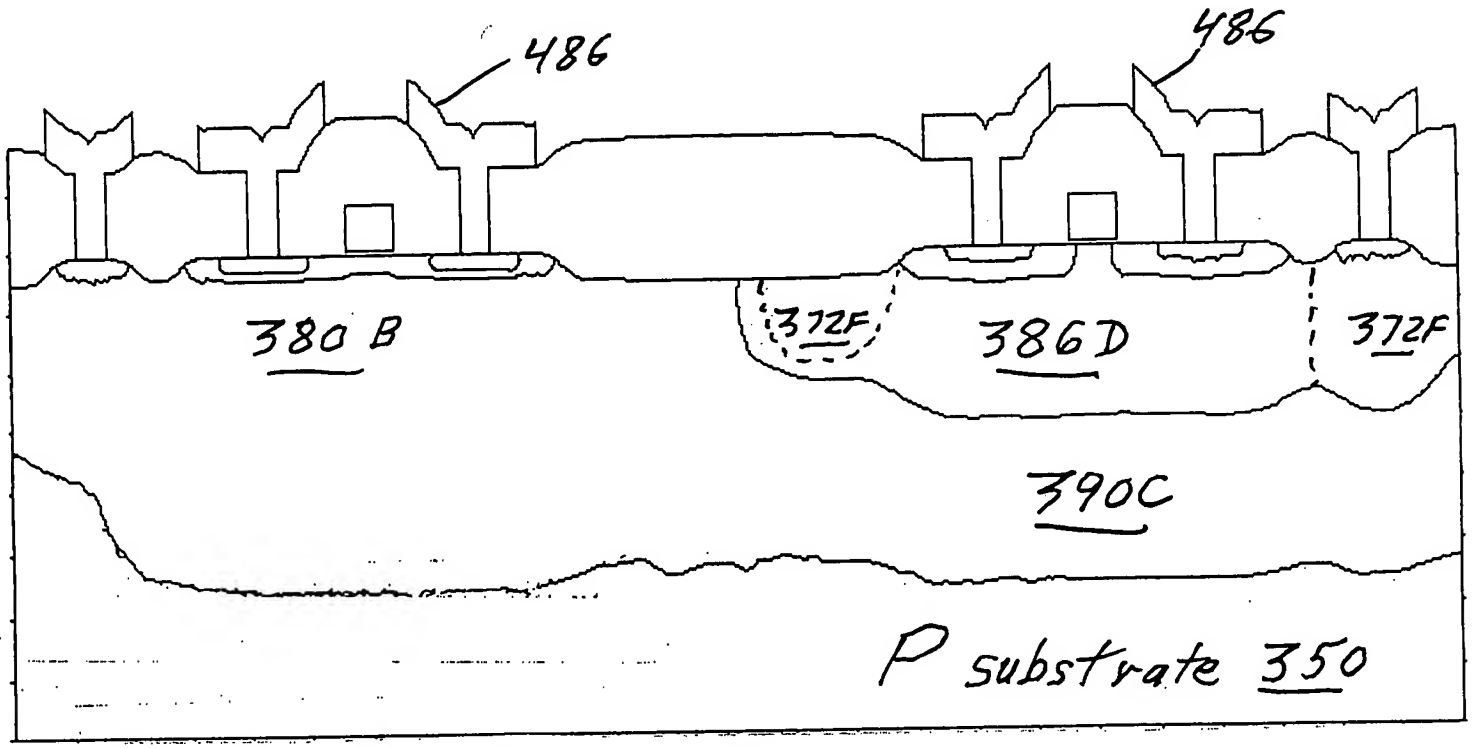

30V Lateral Trench DMOS 308
480
486
486
480
395A
393A
391A
P substrate 350
Metal Layer

Fig. 67D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Metal Layer

Fig. 6E

Fig. 17V

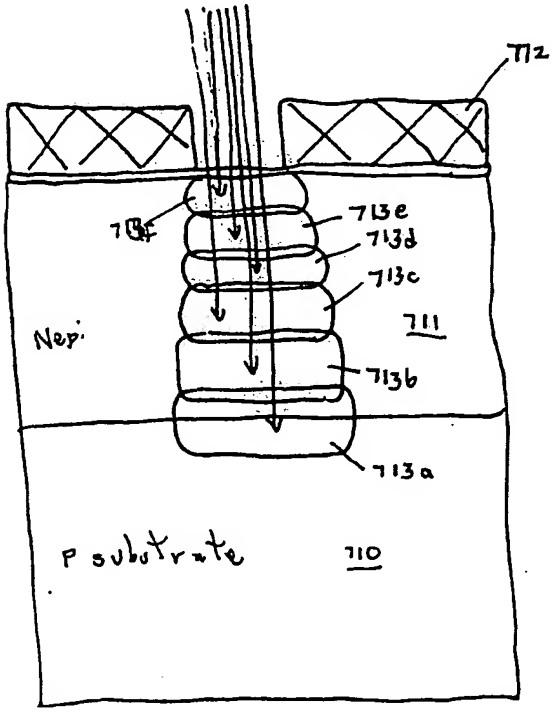


Fig. 17W

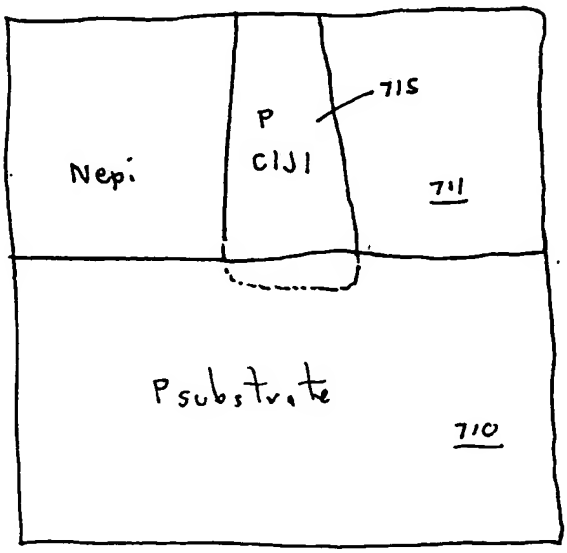


Fig. 17X

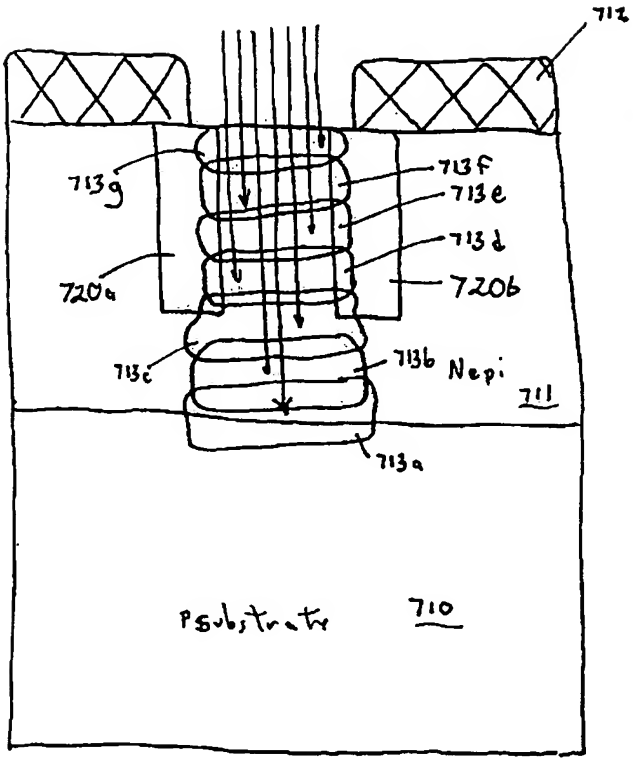


Fig. 17Y

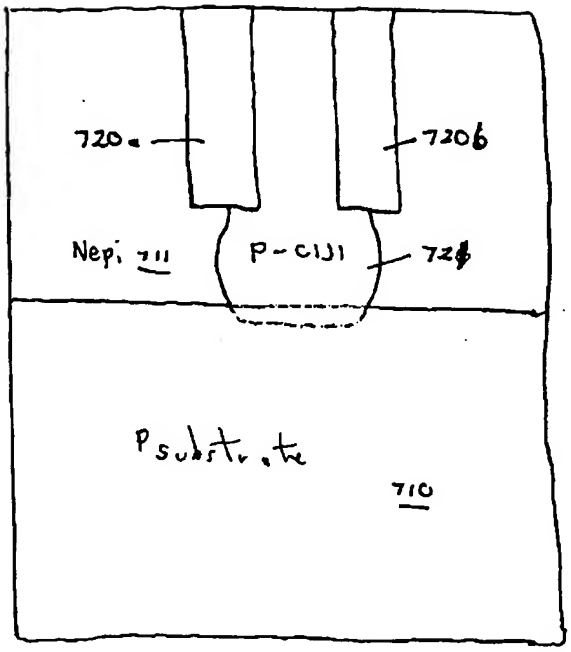


Fig. 17Z

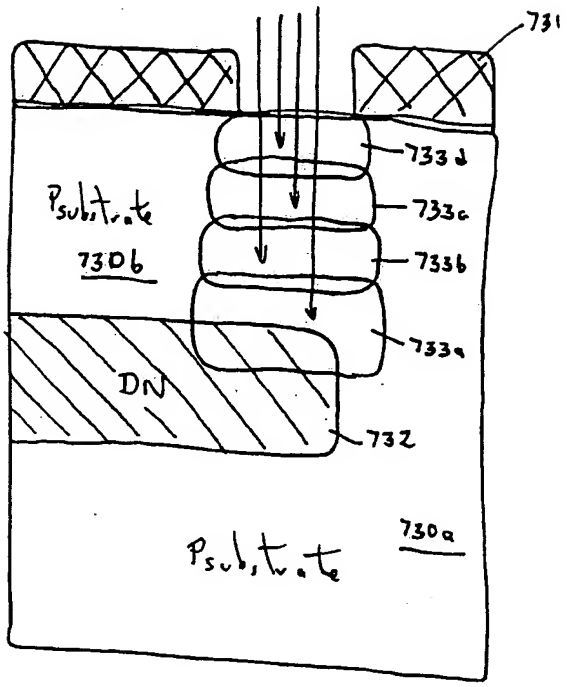


Fig. 17AA

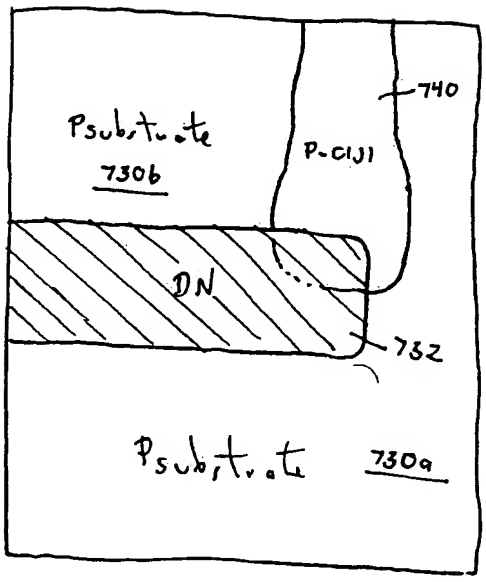


Fig. 17BB

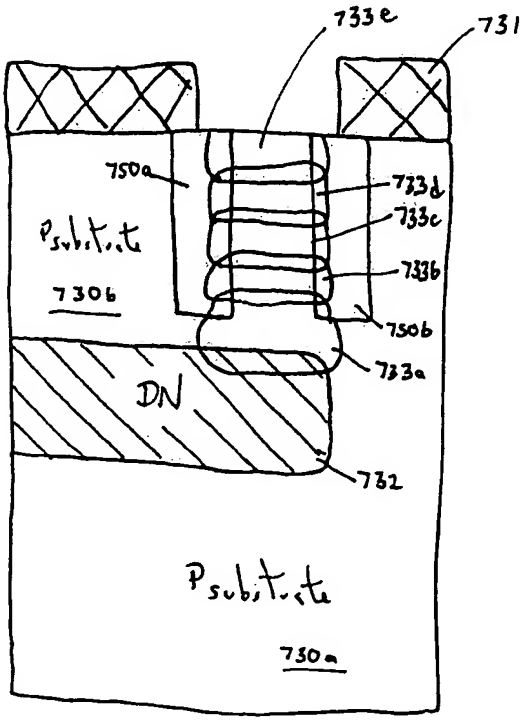


Fig. 17CC